The Open University of Sri Lanka
Department of Electrical and Computer Engineering
Final Examination –2009
ECX 4230 – Fault Diagnosis in Electronic Circuits **(Closed Book)**

Time: 0930-1230hrs. Date: 23.03.2009

Answer any five questions.

1. A transistor amplifier is shown in Figure-Q1.

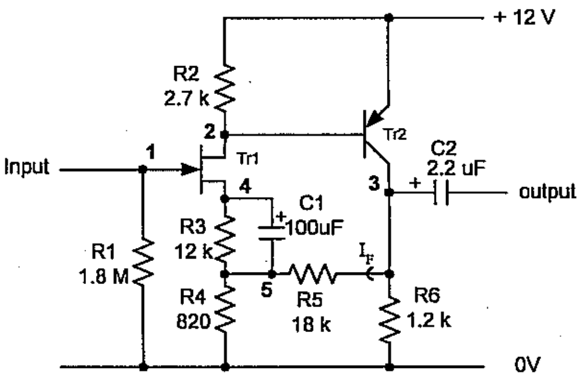

Figure - Q1

The drain current of the transistor Tr1 is given by $I_D = 0.3(V_{GS} - V_P)^2$, where I_D is in mA, V_{GS} is in volts and $V_P = -4V$. You may assume usual notation. The current gain of the transistor Tr2 can be considered as high.

(i) Calculate the current I_F and then find out the voltages at the test points when no signal is applied. Do not assume maximum swing at the output.

(ii) Find out the amplitude of the input signal that will produce an output amplitude of 1V at 1kHz. What is the phase relationship between the input and the output?

(iii) The test point voltages under fault conditions are shown in the following table. Identify the faulty component/s and fault type with reasons.

case	1	2	3	4	5	other
A	0	11.40	6.000	0.270	0.261	no output
B	0	11.40	11.80	3.139	0.201	output clipped
C	0	11.40	0.012	3.077	0.197	no output
D	0	12.00	0	0	0	no output

2. The circuit shown in Figure-Q2 is a Schmitt trigger. Assume that the transistors have high gain and $V_{CE}(sat) = 0$.

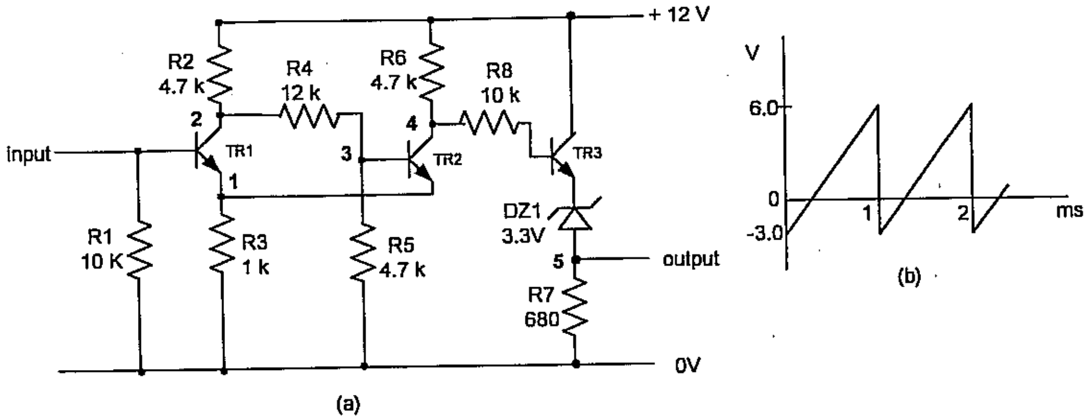

Figure - Q2

(i) Calculate the input voltages at which the output voltage will change.

(ii) Calculate the test point voltages for the input voltages of 3V and 2V respectively.

(iii) The signal shown in Figure-Q2 (b) is applied to the input. Sketch the output waveform with the input to a common time scale and mark the important time and voltage values clearly.

(iv) Determine the faulty component/s in the following fault cases. State the fault type giving reasons. The test point voltages are shown for dc input voltages as indicated.

case	input	1	2	3	4	5
A	2.00	1.400	1.400	1.093	12.00	8.100
B	2.00	2.105	9.390	2.705	2.110	0
C	3.00	2.400	2.410	0.617	9.524	3.580
D	3.00	2.400	9.364	2.636	12.00	8.100

3. A monostable multivibrator circuit is shown in Figure-Q3. The transistors are of high gain type and $V_{CE}(sat) \approx 0$.

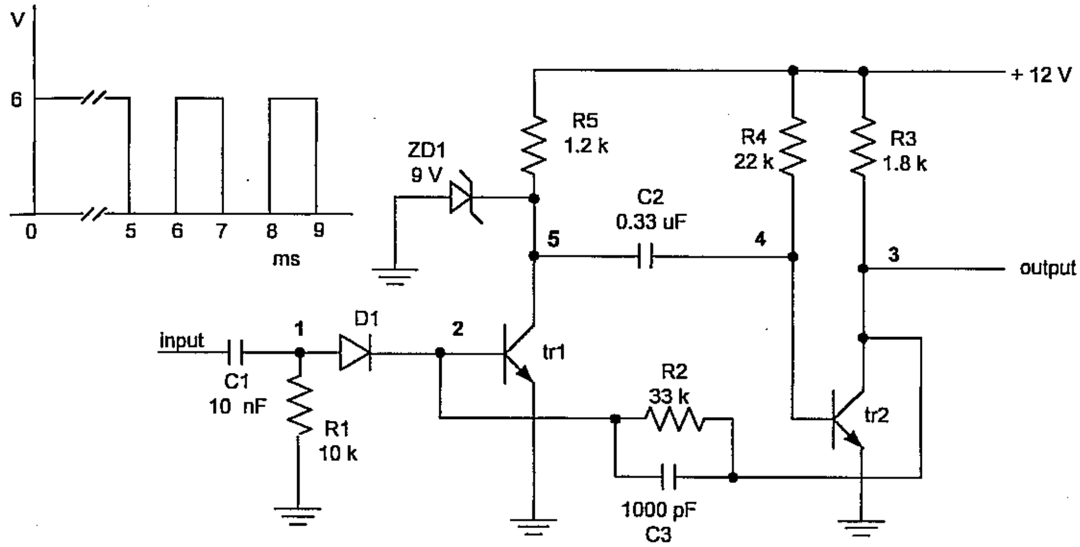

Figure-Q3

(a) Calculate the test point voltages when no signal is applied. If a narrow pulse of 6V is applied to the input, sketch the waveforms at each test point to a common time scale with the input. Mark important voltage and time values related to the waveforms.

(b) If the signal shown in the figure is given to the input, draw the waveform of the output signal using the results obtained in (a). Find the minimum separation between the input pulses in order to generate an output pulse of guaranteed width.

(c) Under fault conditions all test point voltages are observed at no signal. Then some of the test points are observed with an oscilloscope after applying a narrow test pulse. The results are shown in the following table. Find the faulty component/s indicating the fault type giving reasons.

case	1	2	3	4	5	other
A	0	0	0.1	0.6	9.0	very narrow output pulse
B	0	0	0.1	0.6	9.0	dc levels only; at 5&6
C	0	0.6	11.4	0.6	0.1	no output
D	0	0	0.1	0.6	9.0	output pulse height = 6V

4. Consider the amplifier shown in Figure-Q4. The transistors Q1, Q2 and Q3 are of high gain type while the current gain of Q4 is 50.

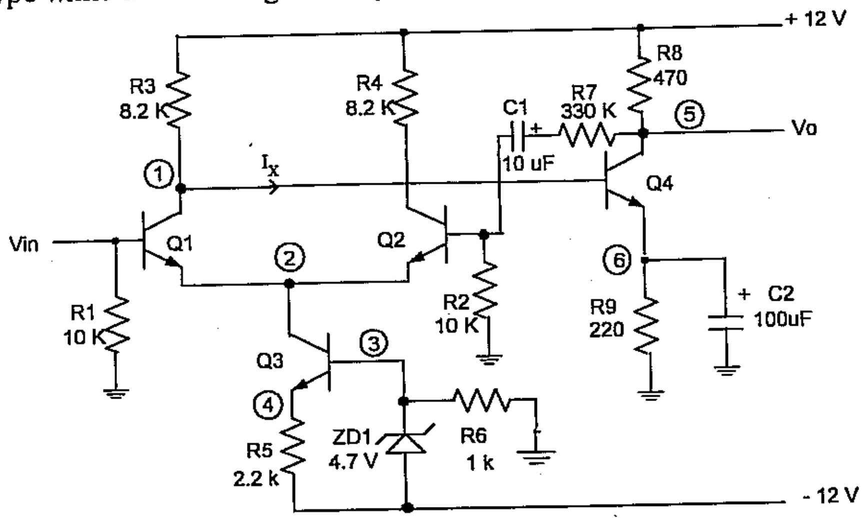

Figure - Q4

(a) Calculate I_X and the test point voltages at no signal. Do not assume any voltage for a test point.

(b) A sine wave signal of 1kHz with 145mV amplitude is applied to the input. Sketch the output signal with the input to a common time scale. Mark the time and voltage values where necessary.

(c) Following table shows the test point voltages under fault conditions. Identify the faulty component/s with fault type giving reasons.

case	1	2	3	4	5	6
A	4.56	0	-7.30	-12.0	4.00	3.96
B	0.50	-0.60	-7.30	-7.90	12.0	0
C	0.70	-0.60	-7.30	-7.90	12.0	0.10
D	0.70	-0.60	-7.30	-7.90	0	0.10

5. Consider the dc voltage regulator circuit shown in Figure-Q5.

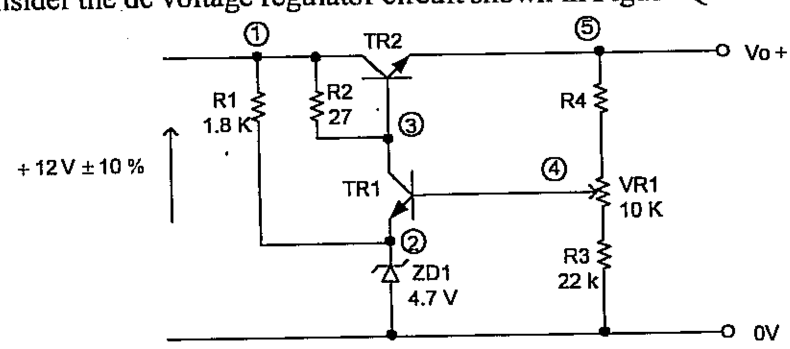

Figure-Q5

Assume that the current gain of Tr2 and V_{CE}(min) is 30 and 1V respectively. The transistor Tr1 is of high gain type.

(i) Find a suitable value for R4 to obtain maximum guaranteed output voltage and calculate it for this value of R4.

(ii) Find the minimum output voltage.

(iii) Calculate the guaranteed maximum load current.

(iv) Calculate the maximum power dissipation in Tr2, R2 and ZD1.

(v) Show the implementation of an active current limit circuit for this power supply and find the component values for the worst case maximum load current.

(vi) Following table shows the test point voltages under fault conditions. Determine the faulty component/s with fault type giving reasons. Assume VR1 is set for the maximum output voltage.

case	1	2	3	4	5	other
A	12.00	4.700	11.82	6.140	11.22	no regulation
B	12.00	4.700	10.28	5.300	9.680	max. load current = 0.9A
C	12.00	4.700	5.900	5.300	5.300	no regulation
D	12.00	4.700	12.00	0	0	no output

6. (a) State the use and limitations of a logic probe.

(b) Consider the digital circuit shown in Figure-Q6.

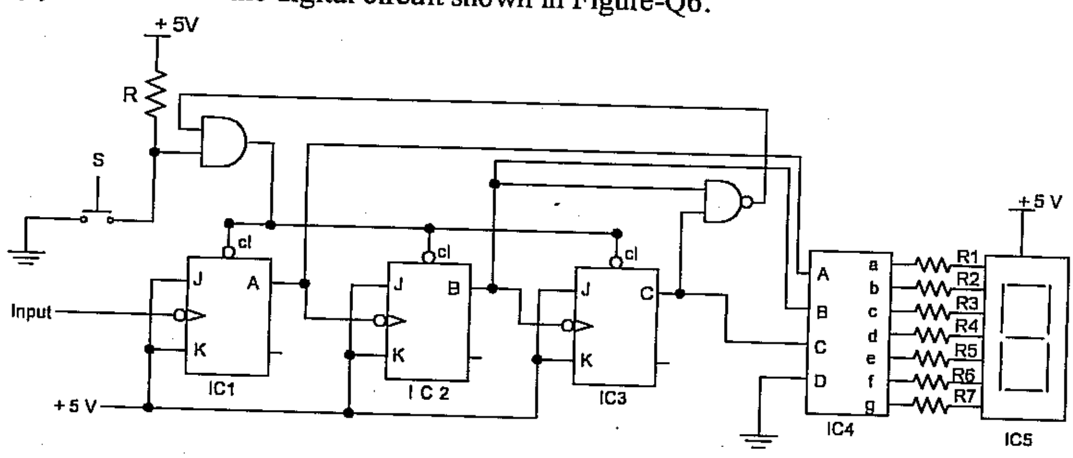

Figure-Q6

(i) Show the operation of the components IC1, IC4 and IC5 with the aid of tables using inputs and outputs.

(ii) After 'S' is pressed, positive pulses of 5V are given to the input. Tabulate the binary states of A, B, C, D and the output of IC5 with each clock pulse.

(iii) State the faulty component/s for the following fault cases giving fault type with reasons.

case	output of IC5
A	2, 3, 2, 3, 2, 3, ...
B	4, 5, 4, 5, 4, 5, ...
C	0, 1, 2, 3, 4, 5, 6, 7, 0, 1, 2, ...

(iv) In a fault case, a logic probe blinks at A, B and C while the output of IC5 is always '3'. State how the logic probe can be used further to determine the exact faulty component.

(v) If the resistor R is open, explain the operation of the circuit.

7. A transistor amplifier used at high frequencies is shown in Figure-Q7(a). The dc current gain of the transistor is 75 and the model of the device is shown in Figure-Q7(b).

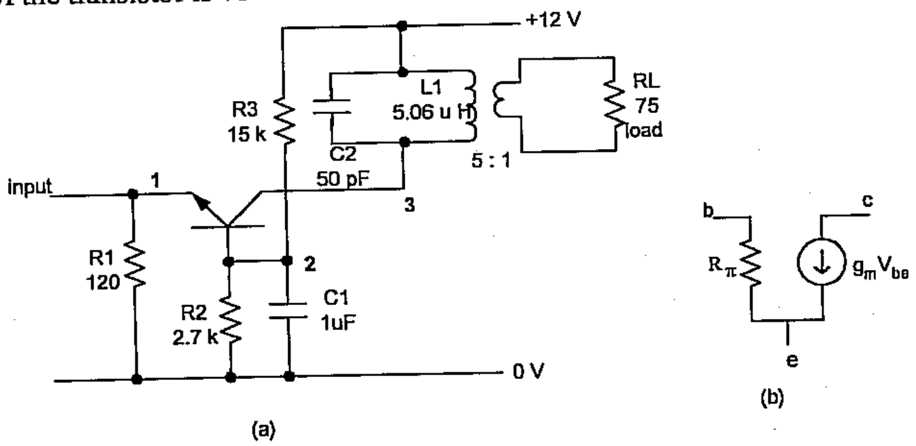

Figure-Q7

(i) Find the base current, the collector current and the test point voltages at no signal.

(ii) Calculate the signal frequency, at which the output signal will be maximum.

(iii) Calculate the voltage gain $\frac{V_3}{V_1}$ at the frequency found in (ii). Hence find the amplitude of the signal at the load if the input signal is 10mV. The value of g_m is 324 $\frac{mA}{V}$ and the value of R_π is not given intentionally.

(iv) Find the faulty component/s giving fault type with reasons for the following faults.

case	1	2	3	other
A	0.061	0.661	12.00	no output
B	11.00	11.60	12.00	-do-
C	0.061	0.661	0	-do-
D	0.985	1.585	12.00	a range of high frequencies is amplified.

8. A lamp flasher circuit is shown in Figure-Q8.

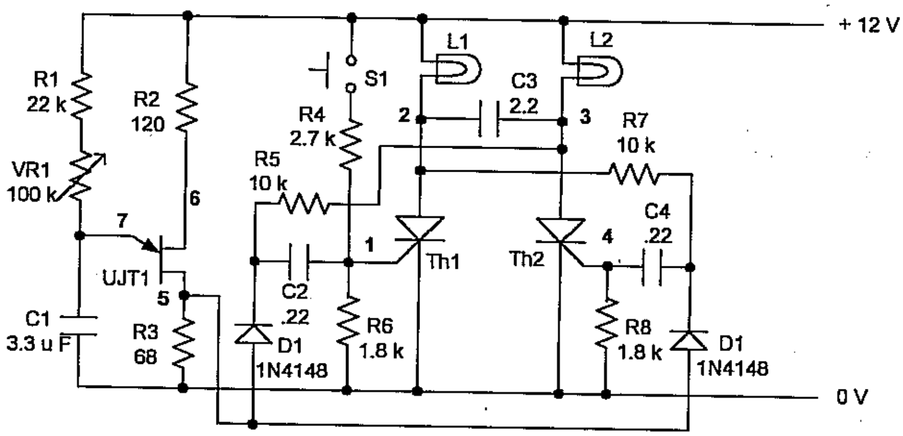

Figure-Q8

(a) Explain the role of S1.

(b) What will happen if C3 is removed?

(c) Calculate the maximum and minimum flash rates if η of the UJT is 0.65.

(d) Following table shows the test point voltages under faulty conditions. Assuming the lamps L1 and L2 are good, find the faulty component/s stating reasons. Note that 'P' indicates pulse or varying voltage.

case	1	2	3	4	5	6	7	other
A	0	1.2	12.0	0	0	12.0	11.8	L1-ON, L2-OFF
B	P	1.2	12.0	P	P	P	P	L1-ON, L2-OFF
C	0	12.0	1.2	P	P	P	P	L1-OFF, L2-ON
D	P	P	P	P	P	P	P	Flash rate low