The Open University of Sri Lanka
Department of Electrical and Computer Engineering
Final Examination - 2008
ECX3230 – Electronics

229

Closed Book Test

Date: 28.03.2009 Time: 14.00- 17.00

Answer any **FIVE** Questions

1 A npn germanium transistor is used in an amplifier circuit, and its characteristics can be considered linear between the limits as shown in the table below. .

I_b(uA)	60		40		20	
V_{CE} (V)	1	10	1	10	1	10
I_C (mA)	2.7	3.2	1.8	2.1	0.9	1.1

a) A 2KΩ resistor is connected between the collector and the positive terminal of a 9V dc supply. The emitter is connected directly to the negative terminal.
   i) Draw the circuit diagram using a fixed bias scheme.
   ii) Sketch the output characteristics and draw the dc load line.
   iii) Determine the quiescent collector emitter voltage and the collector current, if the quiescent base current is 40μA.

b) For a sinusoidal signal, the base current varies with a peak alternating component of 20μA.
   i) Determine the amplitude of the alternating component of the collector current.
   ii) Determine the current gain of the transistor.

2

a) State an application of a Unipolar transistor and a Uni junction transistor.
b) The circuit shown in the Figure 2.1 is using a JFET having I_{DSS} = 16mA and V_p= -4V.

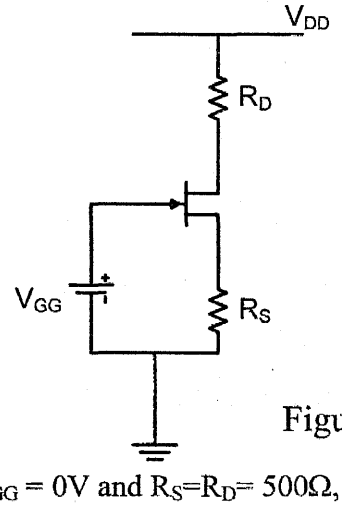


Figure 2.1

If the V_{DD} = 18V, V_{GG} = 0V and R_S=R_D= 500Ω, determine
   i) Gate Source Voltage
   ii) Drain current

iii) Drain Source Voltage
iv) Region of operation of the JFET

c) The circuit shown in Figure 2.2 is an application of a UJT.

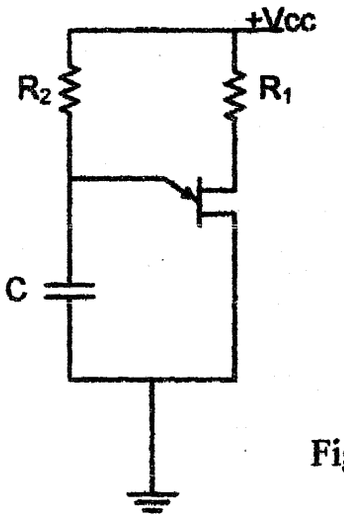


Figure 2.2

i) Draw the equivalent circuit.
ii) Briefly explain the operation of this circuit.

3

a) The circuit given in figure 3.1 is a stabilized dc power supply using a full wave bridge rectifier.

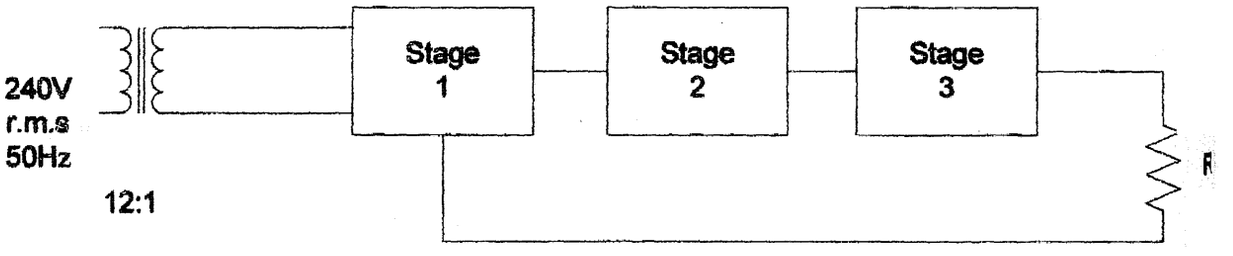


Figure 3.1

i) Write the function of each block in the diagram and draw the relevant circuit for each block.
ii) Calculate the ripple factor of a filter circuit which can be used with Figure 3.1 for the following cases and comment on the results.
(1) For a single capacitor of 1000μF.
(2) For an inductor of 10mH followed by a Capacitor of 1000μF.

b) The circuit of a voltage stabilizer is shown in figure 3.2. A Germanium Transistor with a current gain of 50 is used in this circuit. Maximum power dissipation and the minimum current of the zener diode are 250mW and 5mA respectively.

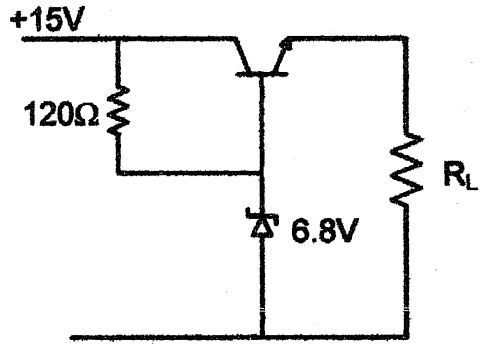


Figure 3.2

i) Calculate the stabilized output voltage.
ii) Find usable current range of the stabilizer.

4 An amplifier using a fixed biased technique is given in figure 4. For the transistor, h_{fe} and h_{ie} are 100 and 1KΩ respectively.

a) Identify the configuration of the transistor?
b) Draw the hybrid parameter equivalent circuits for the following cases.
   i) With C_E.
   ii) Without C_E.

c) Calculate the mid band gain for the cases given in (b).
d) Comment on the results gained in (c).

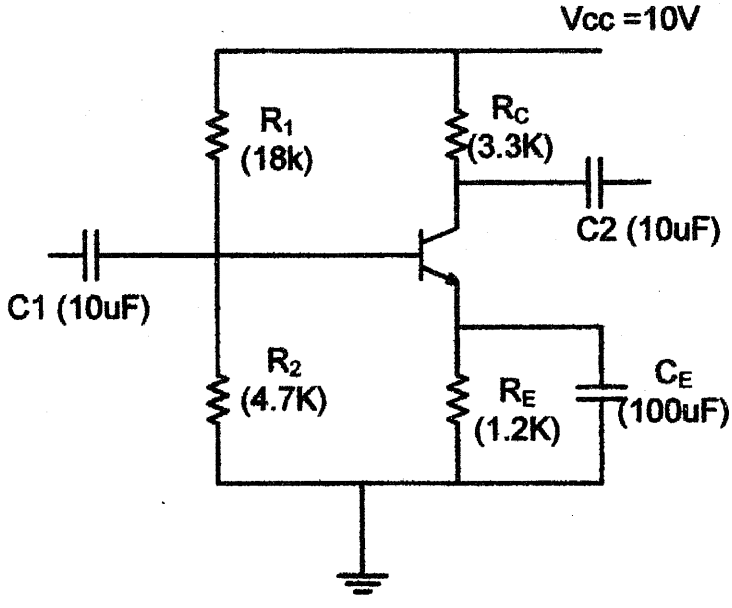
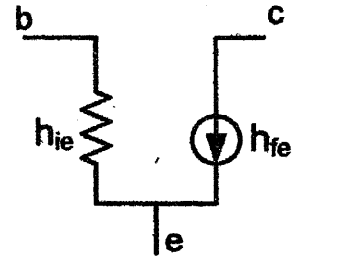


Figure 4



Equivalent model of the transistor

5

a) Obtain the logic function of the circuit shown in figure 5.Tabulate the truth table. Give a single gate which will represent the logic function.

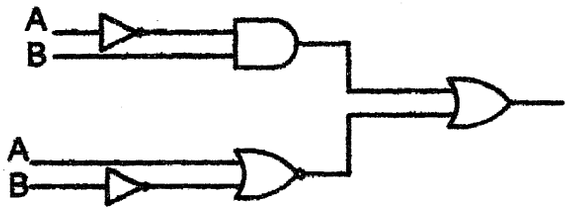


Figure 5

b) **Prove the following identities**
   i) $(P+Q)(Q+S)(P+R)(R+S) = QR+PS$
   ii) $PQ+P\overline{Q}+PQR = P$

c) **Simplify the following using Karnaugh map**
   i) $f(P,Q,R,S) = \sum(0,1,2,4,5,6)$
   ii) $f(P,Q,R,S) = \sum(3,7,12,13,14,15)$

d) **Use minimum number of 2 input NOR gates to implement the logic function obtained in (c)-(i)** above.

6

a) State the advantages of using an Operational Amplifier. The circuit shown in Figure 6 is an application of an Operational Amplifier.

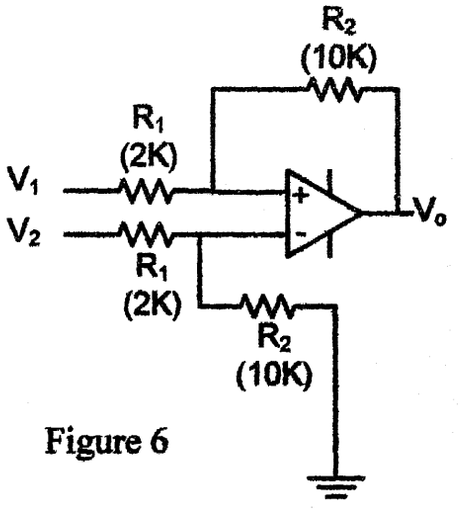


Figure 6

i) Derive an expression for V_O.

ii) Calculate the output voltage of the circuit for the following input voltages.

(a) $V_1 = 1.5$, $V_2 = 0.5$

(b) $V_1 = -2.5$, $V_2 = 0.5$

iii) What is the function of this circuit?

7

a)

i) State the difference between combinational logic circuits and sequential logic circuits.

ii) Tabulate the output Q for all combinations of the input A, B, C of the following circuit.

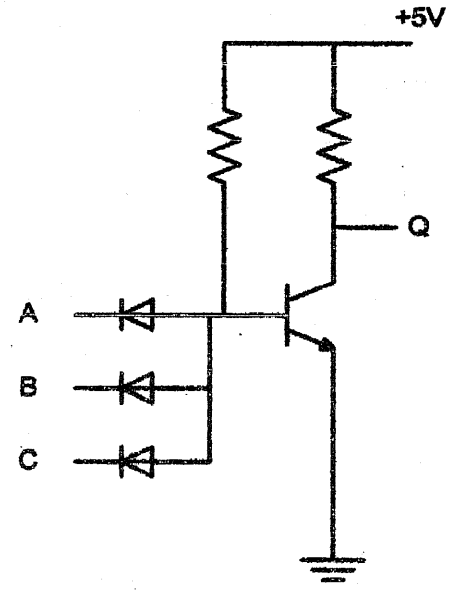


Figure7.1

Assume A, B, C can have only 0V (low) or 5V (high). Diodes are ideal and for the transistor, $V_{CE(Sat)} = 0V$. According to your tabulation what is the logic function implemented by this circuit.

b) A multivibrator circuit is shown in Figure7.2

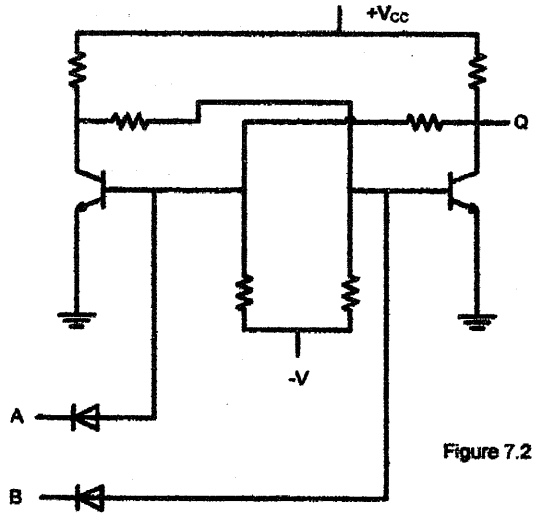


Figure 7.2

i) Tabulate the output Q for all combinations of A and B.
ii) According to the tabulation of Q, what is the function of this multivibrator?

8

a) A 100mH relay coil having a resistance of 10Ω is connected in series with a 50Ω resistance across a 12V battery. The relay operates at 20mA.
   i) Derive an expression for the current /time relationship in the circuit.
   ii) Calculate the time to operate the relay after switching the power.

b)
   i) What do you understand by a clipper and a clamper?
   ii) Sketch the output waveforms of the following circuits shown in Figure8.1and Figure8.2. Also state whether it is a clamper or a clipper.

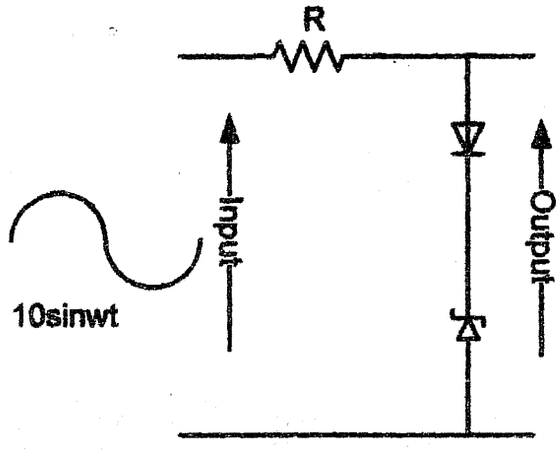


Figure 8.1

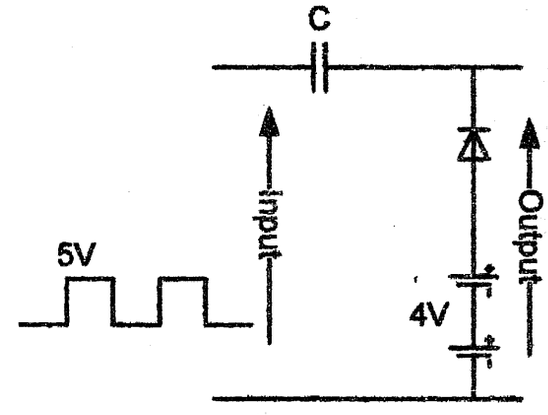


Figure 8.2