00245

The Open University of Sri Lanka
Department of Electrical and Computer Engineering
Final Examination - 2009
ECX3230 – Electronics

Closed Book Test

Date: 05.03.2010 Time: 09.30 – 12.30

Answer any **FIVE** Questions

1)

a) A Germanium diode when forward biased at 25^0C carries a 2mA current at 0.3V. Assume V_T is 25mV at 25^0C.

i) Calculate the diode current when this diode is reversed biased by 10V.
ii) Find the diode current when the diode is forward biased and at a temperature of 50^0C.(η=1 for Ge)

b) A certain PN junction was designed to use as a voltage controlled capacitor which is shown in Figure 1.1. Ohmic resistance and reverse diode resistance of the designed diode is negligible.

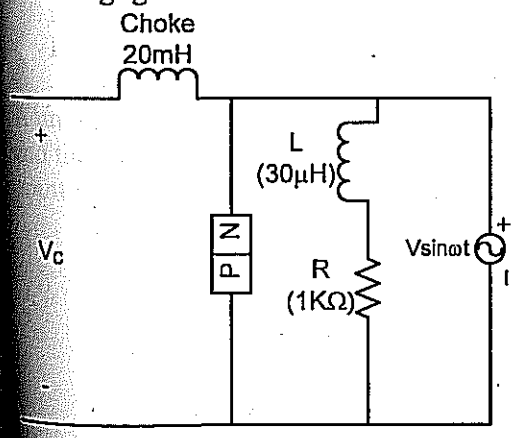

Figure 1.1

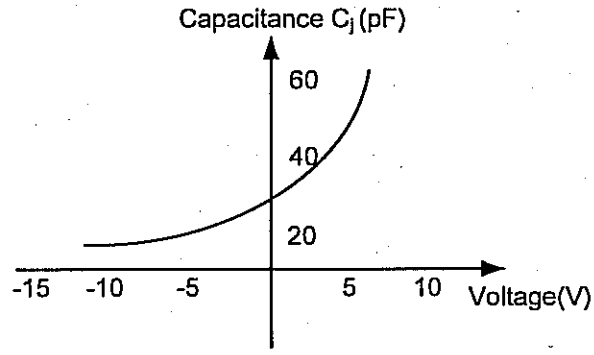

Figure 1.2

i) Derive an expression for the resonance frequency of the circuit in Figure 1.1.
ii) Calculate the capacitance of the designed diode if the circuit resonates at 25 MHz.
iii) What is the required voltage for this circuit to resonate?

2) A common emitter transistor amplifier is shown in Figure 2.1. Transistor is silicon and its current gain is 50.

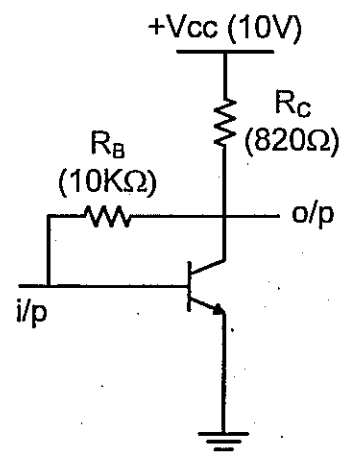

Figure 2.1

a) Draw the D.C load line.
b) Find the base current at Q point.
c) Mark the Q point on the load line.
d) What is the maximum possible value of the undistorted output signal?
e) Derive an expression for the stability factor for the circuit given in Figure 2.1.
f) Calculate the stability factor.

3)

a) State De Morgen's theorem for three Boolean variables A, B, and C.
b) Simplify the following logic functions using Boolean algebra.
   i) $X1 = \overline{A+B} \cdot \overline{ABC} \cdot \overline{\overline{A}C}$
   ii) $X2 = \overline{A}BC + \overline{A}\overline{B}C + \overline{A}B\overline{C} + ABC + AB\overline{C}$

c) The input to a combinational logic circuit is a 4 bit binary number ABCD. Where D is the least significant bit. The output of the circuit will be high when the input satisfies the following conditions ;

   Odd numbers that are greater than 2 and the remainder is not equal to 1 when divided by 5

   Or

   Numbers that are greater than 9 and should not be divisible by 3.

   i) Draw the truth table and the Karnaugh map for the output function.
   ii) Minimize the logic function for the output using the Karnaugh map and implement it using two input NAND gates.

4) A regulated dc power supply is shown in Figure 4. The transistor and diodes are made of silicon semiconductor. A minimum current of 1 mA is required to operate the zener diode and its worst case power dissipation in this circuit is 25mW.

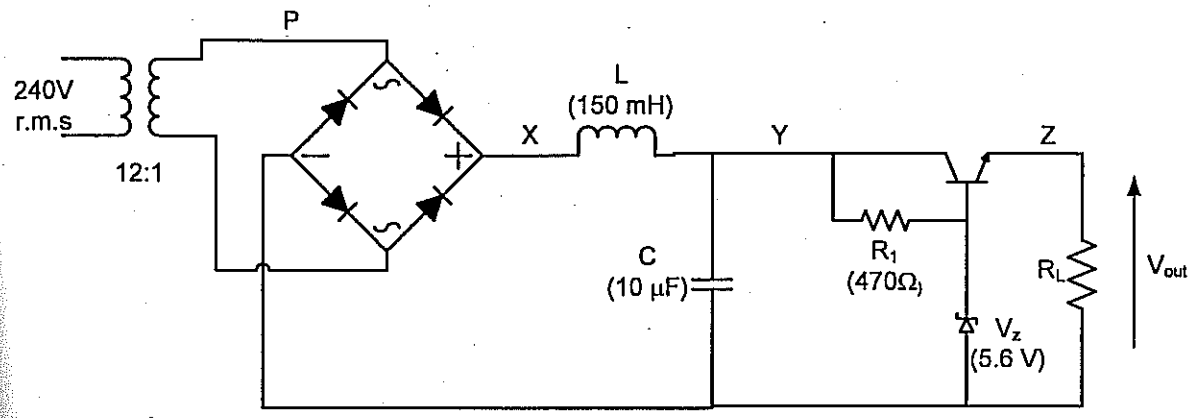

Figure 4

a) Identify and name the main functional blocks.
b) Explain the operation of the block in between points Y and Z.
c) Calculate, the
   i) Voltages at P, X, Y, Z.
   ii) Current range of the output, if current gain of the transistor is 30.
   iii) Voltage regulation of the circuit (Figure 4) at full load.

5) A unipolar transistor amplifier is shown in Figure 5. The drain current is 10mA at $V_{GS} = 0$ and the pinch off voltage of the device is -3V. The circuit to be designed so that the quiescent point is at $I_D = 5mA$ and $V_{DS} = 5V$.

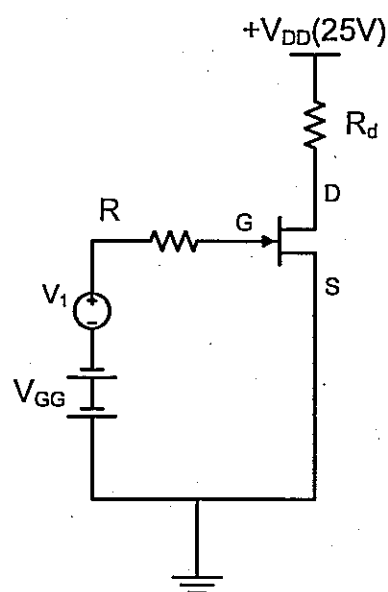

Figure 5

a) Calculate the gate voltage and R_d resistance.
b) Draw the small signal equivalent model for Figure 5.
c) Derive an expression for the voltage gain of the amplifier and calculate it.

6)

a) An Operational amplifier circuit is shown in Figure 6.1.

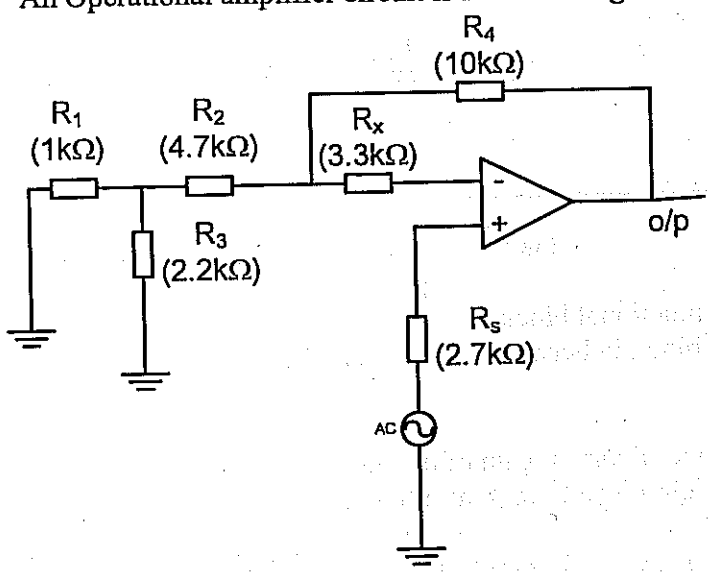

Figure 6.1

i) Derive the voltage gain of this circuit.
ii) If the input voltage is 2sinωt, find the output voltage.
iii) Sketch the output signal with reference to the input signal.
iv) State the function of this circuit.

b) A half wave rectifier circuit using a SCR is shown in Figure 6.2. Triggering signal fires SCR after π/6 rad from each zero crossing of a cycle.

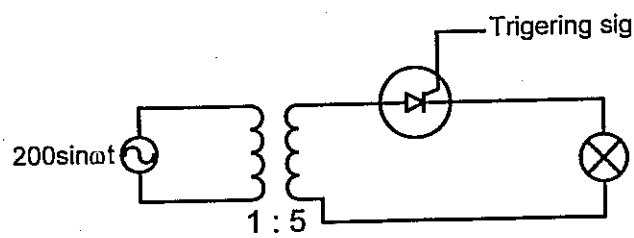

Figure 6.2

i) Determine the mean load voltage. (Prove any formula you use.)
ii) What is the effect, when the triggering angle is changed to π/3?
iii) If the SCR is replaced with a Traic comment on the operation of the circuit.

7) An impendence matching circuit is shown in Figure 7. For the transistor, h_{ie},h_{re}, h_{fe} and h_{oe} are 2.2KΩ, 0, 50 and ∞ respectively.

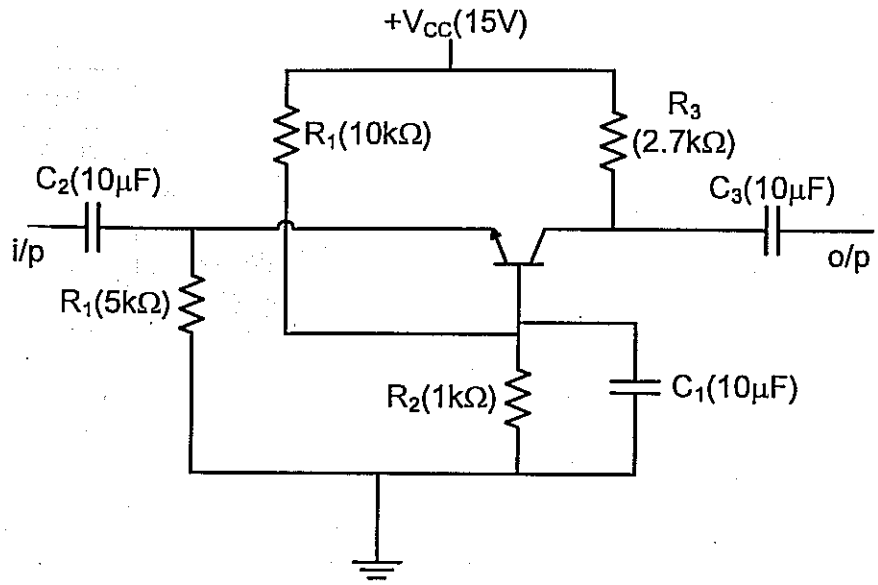

Figure 7

a) Identify the configuration of the transistor.
b) Draw the hybrid parameter equivalent circuit.
c) Derive expressions for the
   i) Voltage gain
   ii) Current gain
   iii) Input impedance
   iv) Output impedance
d) Calculate the values of the quantities shown in (c).
e) Give a practical application of this circuit.

8)

a) An astable multivibrator circuit is shown in Figure 8. Both transistors are matched to each other.

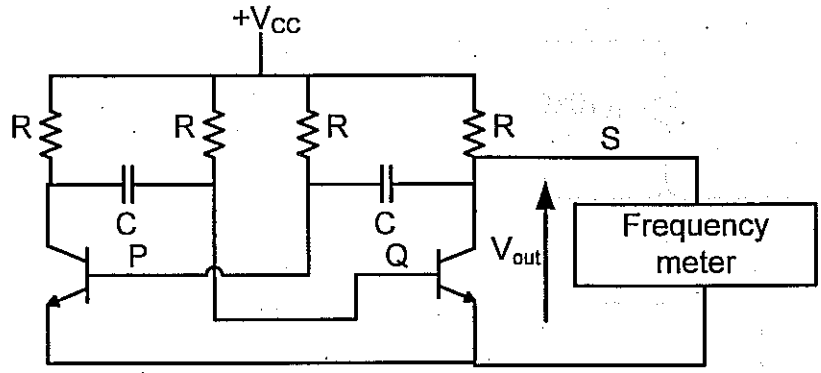

Figure 8

i) What are the operating regions of the transistors?
ii) Sketch the waveforms at point P,Q and S
iii) Calculate the output frequency, if V_{CC}, R and C are 10V, 5kΩ and100μF respectively.

b) A student needs to design an asynchronous decade (decimal 10) counter. It is required to use JK flip flops and NAND gates to build the circuit.

i) How many flip flops are required to build the circuit?
ii) Draw the circuit diagram of the counter.
iii) If the input is a 5V/1kHz square wave signal, draw the output signal of each flip flop and the input to a common time scale.