THE OPEN UNIVERSITY OF SRI LANKA
FACULTY OF ENGINEERING TECHNOLOGY
DIPLOMA IN TECHNOLOGY – LEVEL 3
FINAL EXAMINATION 2007/2008

MEX3272 – APPLIED ELECTRONICS

DATE : 24th APRIL 2008
TIME : 0930 HRS. – 1230 HRS.
DURATION : THREE (03) HOURS

INSTRUCTIONS

- *Question paper consists of **eight** questions. Answer **only five** questions.*
- *All questions carry equal marks.*

Question 01

(a) State the Thevenin's theorem and Norton's theorem.

(b) i. Convert the following Thevenin equivalent circuit in figure Q1 (b-i) to Norton equivalent circuit.

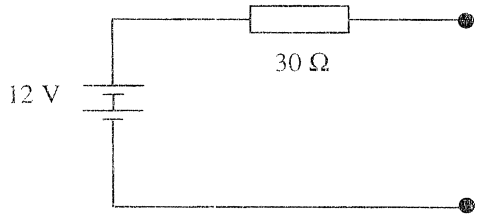

Figure Q1 (b-i)

ii. Convert the following figure Q1(b-ii) Norton equivalent circuit into a Thevenin equivalent circuit.

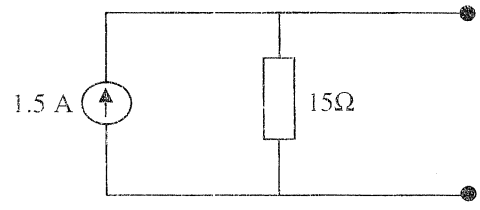

Figure Q1 (b-ii)

(c) Following figure Q1(c) represents a two port network consisting of two voltage sources and three linear resistors. (r_1 and r_2 are the internal impedances of the voltage sources and R_L is load resistance)

i. Find the Thevenin equivalent circuit.
ii. Find the Norton equivalent circuit.
iii. Using Thevenin's theorem find an expression for the current through the load resistor $\mathbf{R_L}$.

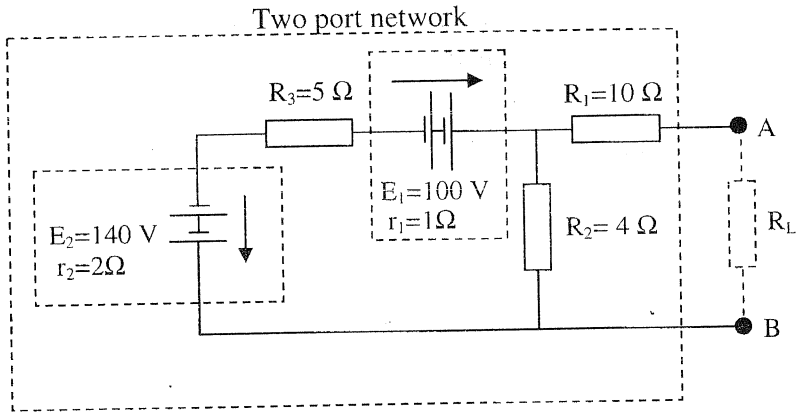

Figure Q1(c)

(d) A delta connected source has voltages given by

$V_{ab}=1000\angle 30^0$ $V_{bc}=1000\angle -90^0$ $V_{ca}=1000\angle 150^0$

This source is connected to a delta connected load consisting of 50Ω resistances. Find the line currents and the power delivered to the load.

Question 02

(a) Find R_{load} for maximum power dissipation in the circuit shown in figure Q2 (a).

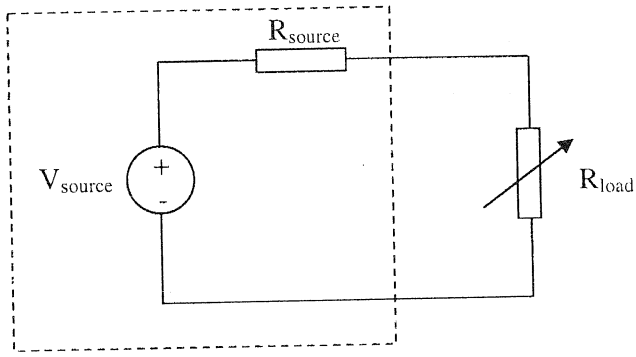

Figure Q2 (a)

(b) In the following figure Q2 (b), the source is connected to the RC circuit by a switch that closes at t=0.Assume that initial voltage across the capacitor just before the switch closes is V_c (0.) = 0.Find the voltage across the capacitor as a function of time. (***Hint:*** Apply **KCL** for node **A**)

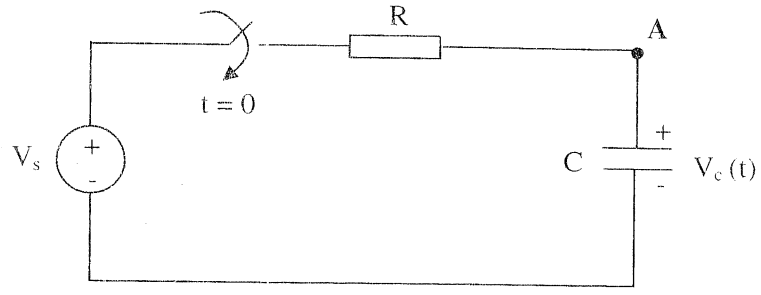

Figure Q2 (b)

(c) Calculate V_c when t=0, RC, 2RC, 3RC, 4RC, 5RC. Give your comments about the voltage across the capacitor when t=5RC.

(d) A series combination having R = 2MΩ and C = 0.02μF is connected across a DC voltage source of 100V. Determine,

i. Time constant of the circuit
ii. Capacitor voltage after 0.02 s,0.1 s and 2 hours
iii. Charging current after 0.02 s,0.04 s and 0.1 s

Question 03

(a) Draw a circuit symbol of a diode and a zener diode.

(b) What are the full wave rectification methods, explain it using circuit diagrams.

(c) List the biasing techniques of a transistor.

(d) Following figure Q3 (d) shows the emitter follower regulation circuit. Calculate the values of V_L, I_L, V_{CE} and power dissipated by T_1.Assume that the transistor is ***Si***.

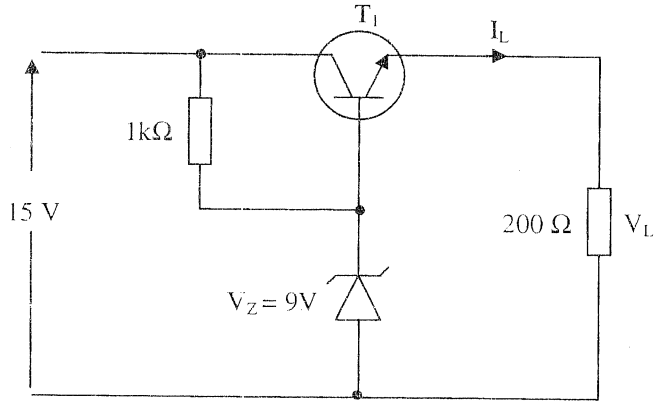

Figure Q3 (d)

Question 04

(a) Write down the three BJT configurations, and draw circuit diagrams to show each of them using a npn transistor.

(b) Draw the input and output characteristics of a BJT for CE configuration.

(c) List three applications of a transistor and briefly explain each of them.

(d) Consider the common emitter transistor amplifier as shown in figure Q4 (d).
Where: V_{CC}=12V, V_{BE} = 0.6V, R_1=15kΩ, R_2 = 2.7kΩ, R_C = 1kΩ, R_E = 220Ω, β = 100

i. Using Thevenin's equivalent circuit, calculate the quiescent voltages and currents.
ii. Is this amplifier non-inverting or inverting?
iii. Find the small signal mid band voltage gain.

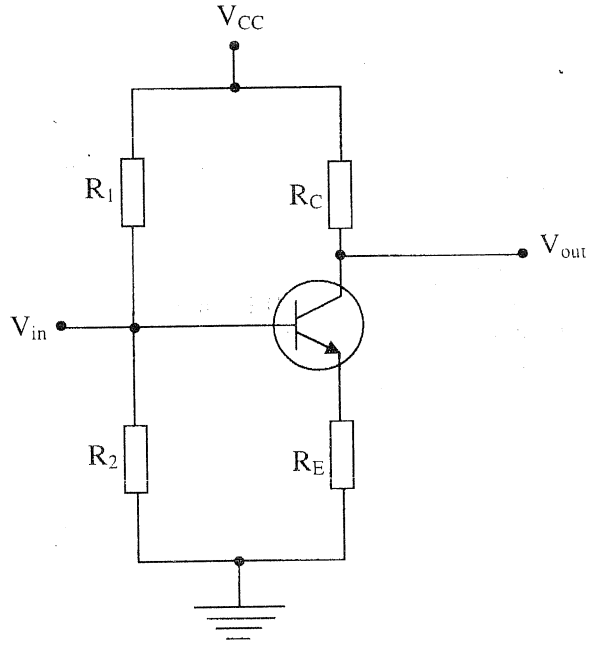

Figure Q4 (d)

Question 05

(a) List four characteristics of an ideal operational amplifier (Op-Amp). Compare the ideal values with its typical values.

(b) Explain following terms of an operational amplifier

i. Input bias current
ii. Output offset voltage
iii. Common Mode Rejection Ratio (CMRR)
iv. Slew rate.

(c)

i. What are the benefits of **negative feedback** (Degenerative feedback) in an Op-Amp circuit?
ii. Why is it necessary to reduce the gain of an op-amp from its open loop gain?
iii. What do you mean by the term "**Virtual ground**"?
iv. Derive an equation for the closed loop voltage gain for a non-inverting amplifier.
v. What is a voltage follower? Explain it using a circuit diagram and find the voltage gain of it?

(d) Determine an expression for the output voltage V_{out} in the circuit shown in figure Q5 (d). Assume that the operational amplifier is ideal.

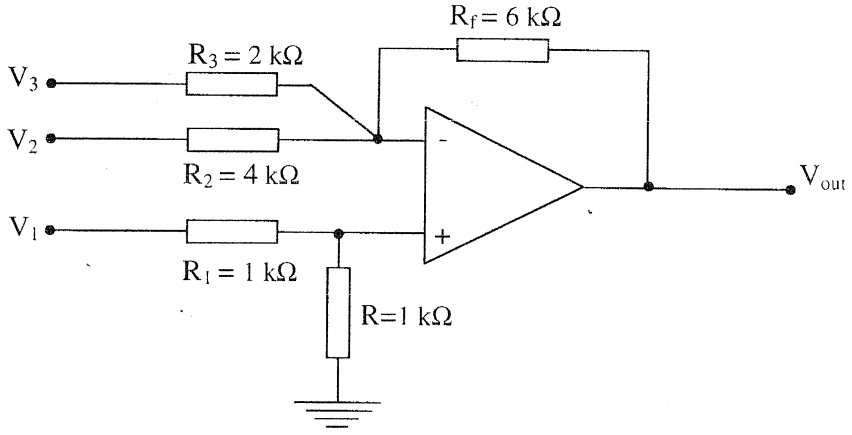

Figure Q5 (d)

If V_2=3V and V_3=2V, then find the value of V_1 to get V_{out} = 0 V.

Question 06

Explain the following terms using diagrams and mention one application for each of them.

i. SCR
ii. LDR
iii. Triac
iv. Opto coupler
v. Thermo couple

Question 07

(a) i. Convert 10001111_2 to Octal and Hexadecimal

ii. Represent -96_{10} in
   a. Sign magnitude method
   b. 1's compliment method
   c. 2's compliment method

(b) i. State De Morgan's theorem for two Boolean variables A and B.

ii. Define the following 2-input device.

a. NAND gate
b. Exclusive OR gate

iii. Realize an Exclusive OR gate using only NAND gates.

(c) Simplify the following logic functions using Boolean algebra.

i. $\overline{A}\overline{C} + B\overline{C} + \overline{A}BC + ABC$

ii. $A\overline{B}\overline{D} + AB\overline{C}\overline{D} + ABC\overline{D} + \overline{A}\overline{B}\overline{D} + \overline{A}BC\overline{D}$

(d) A, B, C, D are four inputs of a circuit, representing binary values from 0000 to 1111 (i.e. 0 to 15). The input A is MSB and D is LSB. The out put of the circuit (F) is **true**, if the input is divisible by 4, 5, 6 or 7 with the exception of 15, otherwise the output is **false.** Assume that zero is not divisible by any number.

i. Write the Boolean expression for the output (F) and simplify it using Karnaugh map, Show the steps very clearly.
ii. Design a circuit using logic gates (OR, AND and NOT) to carry out the function.

Question 08

(a) Explain briefly the terms "Combinational-logic" and "Sequential-logic".

(b) Define,

i. JK edge-triggered Flip-Flop
ii. SR edge-triggered Flip-Flop
iii. Construct D edge-triggered Flip-Flop using a JK Flip-Flop and a NOT gate.

Give circuit diagrams, truth tables for each of them

(c) i. What is the,

a. Resolution,
b. Full scale error,
c. Linearity error, of a **DAC** (Digital to Analog Converter)

ii. Give three applications of a DAC.

iii. A 4-bit weighted resistor DAC has a $V_{ref} = 12V$ and a feedback resistor (R_f) = R. Find the resolution and the full scale analog output current.

(d) Design a 3-bit **Gray Code** synchronous counter using JK Flip-Flop and logic gates. You have to show the state diagram, state table, K-map, logic expressions and the circuit implementation very clearly.