The Open University of Sri Lanka
Department of Electrical and Computer Engineering
Diploma in Technology Level 03

ECX3230 – Electronics
Final Examination **Closed Book Test**

Date: 23rd April 2008 Time: 09.30-12.30

Answer any **five** questions.

1. Figure-Q1A shows a single stage transistor amplifier which makes use of a simple biasing arrangement. Figure-Q1B shows the output characteristics of the above transistor.
   (a) Explain the functions of R_B, R_C and R_L.
   (b) Calculate the base current I_B.
   (c) Draw the dc load line on figure-Q1B. (Use the given answer sheet)
   (d) Locate the operating point of the transistor on figure-Q1B and find V_{CE} and I_C at the operating point.
   (e) Now a sinusoidal signal is applied to the input of the amplifier and the signal amplitude is gradually increased. What is the maximum possible value of the undistorted output voltage?

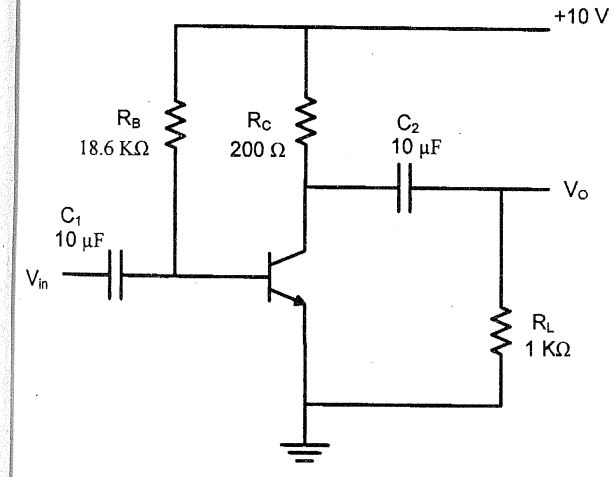

Figure – Q1A

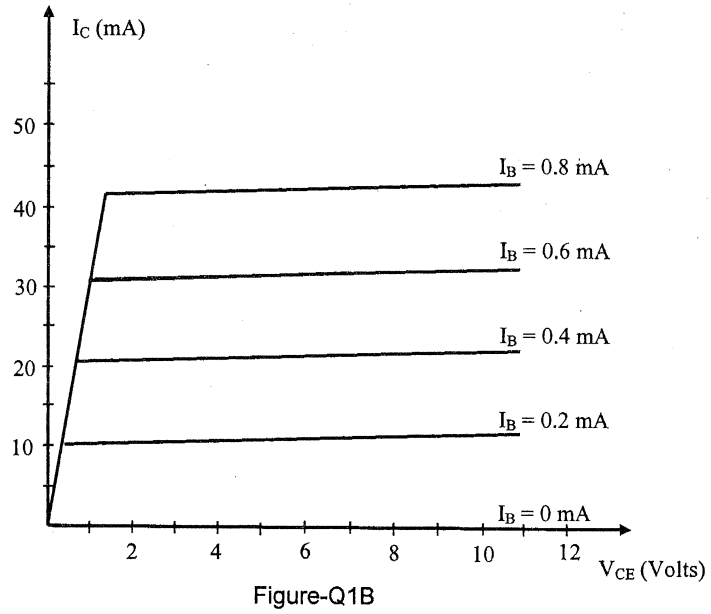

Figure-Q1B

2.
   (a) Write down the advantages of field effect transistors (FETs) over bipolar junction transistors (BJTs).
   (b) Consider the circuit shown in figure-Q2.

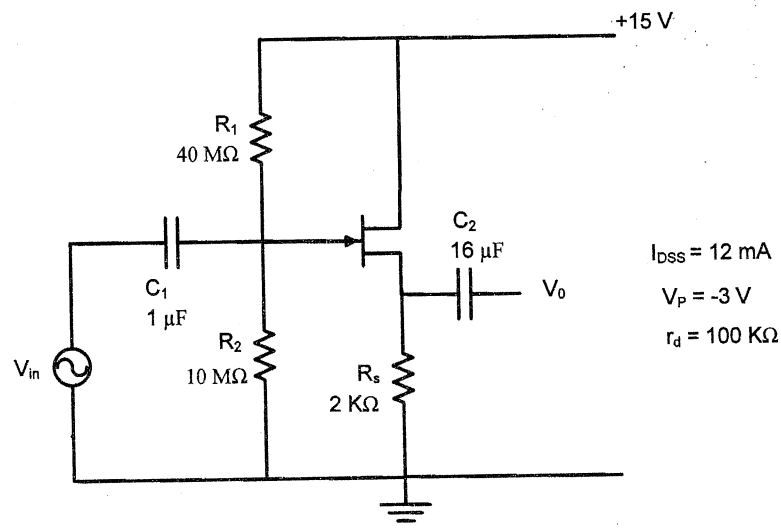

Figure - Q2

4.

i. What is the amplifier configuration used in this circuit?
ii. Find the current I_D when no input signal is applied.
iii. Find the g_m of the device under the operating conditions given in part (b).
iv. Draw the AC equivalent circuit for the amplifier and derive expressions for the voltage gain and input impedance for mid band frequencies.
v. Calculate voltage gain and input impedance. Assume that the reactance of the capacitors is negligible.

3.

(a) Indicate the transistor configurations that exhibit the following properties.
i. Highest input resistance
ii. Highest voltage amplification
iii. Lowest output resistance
iv. Highest current amplification

(b) A transistor amplifier is shown in figure-Q3A.

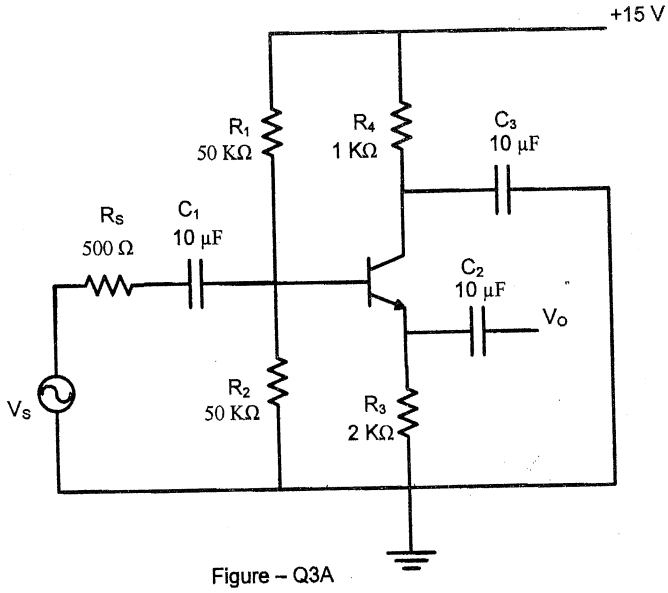

Figure – Q3A

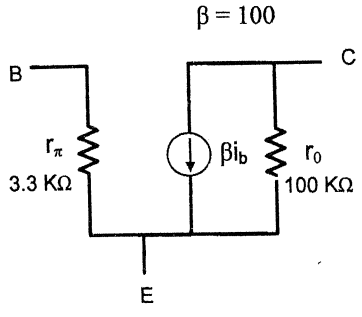

Figure – Q3B

5. A simple dc power supply circuit is shown in figure-Q5.

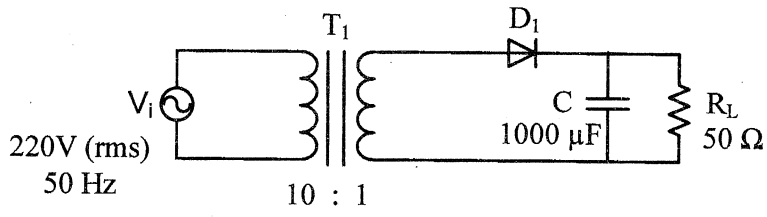

Figure-Q5

(a) Identify the type of this rectifier circuit.
(b) Sketch the voltage across R_L as a function of time showing its relationship to the secondary voltage from the transformer.
(c) Calculate the peak secondary voltage from the transformer T_1.
(d) Assuming 10% ripple voltage across the load calculate the peak to peak amplitude of the ripple voltage.
(e) Explain how the circuit could be modified to produce a 5% ripple voltage.

8.

6.

(a) Figure-Q6A shows a D latch circuit. Write the truth table indicating E, D, Q and $\overline{Q}$ for the circuit.
(b) Show how this D latch can be used to form a gated SR latch and give its truth table.
(c) The waveforms of figure-Q6B are applied to the D and E inputs of figure-Q6A. Draw the timing diagrams of the waveforms Q and $\overline{Q}$ with D and E inputs. Assume Q = 0 initially.

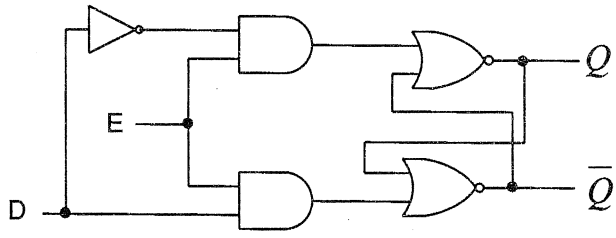

Figure – Q6A

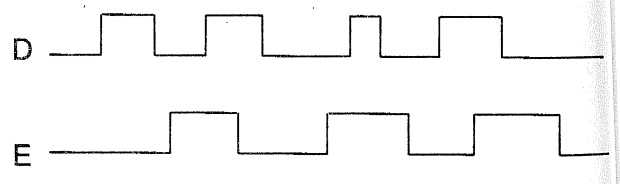

Figure-Q6B

7.

(a) Obtain the logic function Z of the circuit shown in figure-Q7 in the sum of products form and then derive the truth table for the circuit.
(b) Find the minimized solution of the following function in sum of products form using the karnaugh's map.
$F = \Sigma\ 0, 1, 2, 3, 4, 5, 8, 10, 11, 14$
(c) Design a logic circuit with inputs P, Q, R so that output S is HIGH whenever P is 0 or whenever Q = R = 1.
(d) Implement the design of part (c) using only NAND gates.

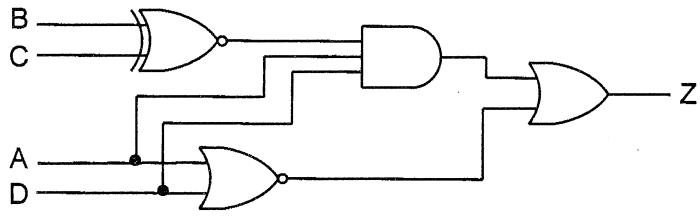

Figure – Q7

8. A multivibrator circuit is shown in figure-Q8.

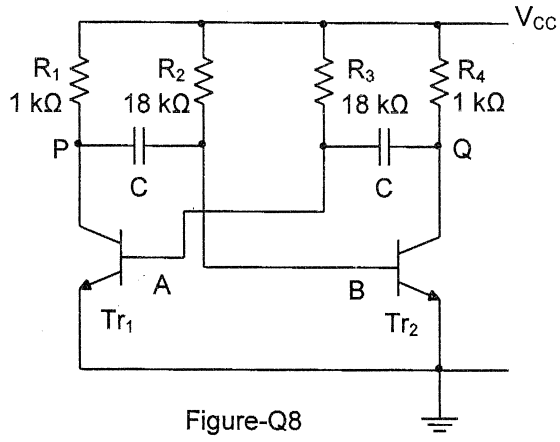

Figure-Q8

(a) What is the type of this multivibrator?
(b) Draw the waveforms at points A, B, P and Q in a common time scale. Assume that at time t = 0, Tr_1 is switched on.
(c) Derive an expression to find the frequency of the waveform at point Q.
(d) The multivibrator shown in figure-Q8 is designed to give a symmetrical output waveform having a periodic time of 2 ms. Calculate the value of C.

Answer Sheet for Question 1

Attach this answer sheet to your answer script if you answer for question 1.

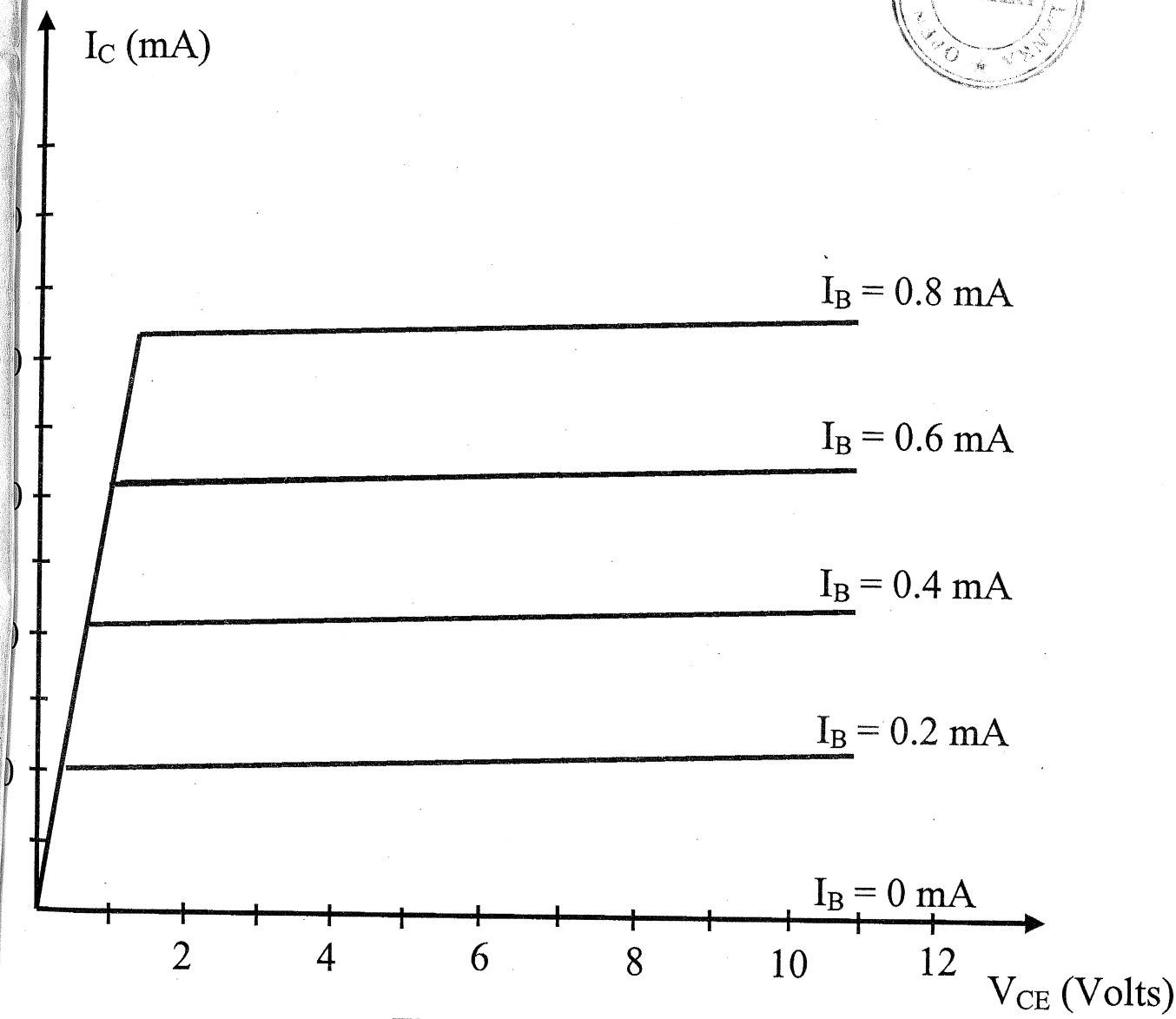

Figure-Q1B