THE OPEN UNIVERSITY OF SRI LANKA
Faculty of Engineering Technology
Department of Electrical & Computer Engineering

Bachelor of Software Engineering Honours

Final Examination (2016/2017)
ECX5263: Computer Organization and Operating Systems

Date: 23rd of November 2017 (Thursday) **Time: 9:30 am –12:30 pm**

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1. This paper contains eight (8) questions in two Sections. Answer any five (5) questions at least two (2) questions from each section. All questions carry equal marks.
2. Assume reasonable values or any suitable assumptions for any data not given in or if any doubt as to the interpretation of the wording of a question. Clearly state such assumptions made on the script.
3. You are allowed to use scientific calculators during the exam.
4. You are NOT allowed to use any study material or any other electronic resource during the examination.

Section A
Answer at least **two (2)** questions from this section.

Q1.

a) What is an I/O system? State **three** major tasks of an I/O system?

[04 Marks]

b) Briefly describe Programmed I/O, Memory mapped I/O. Interrupt I/O and Co-Processor I/O with diagrams

[04 Marks]

c) Find the efficiency of a processor that has following Programmed I/O system, Instruction execution rate – 0.15 MIPS, Number of instructions that needed by I/O subroutine to write to a disk – 10,000

[06 Marks]

d) Assume that an Interrupt I/O is added to the processor given in question (Q1.c) and now disk has total latency of 100ms. Initiating the disk transfer and respond to the interrupt at the end of the disk latency requires 200 instructions. Find the useful time and the efficiency of the system.

[06 Marks]

Q2.

a) Briefly describe the Flynn's classifications (SISD, SIMD, MISD, MIMD) on computer organization giving block diagrams for each organization.

[04 Marks]

b) Describe RISC and CISC architectures providing advantages and disadvantages of each architecture.

[04 Marks]

c) An instruction pipeline has five stages and the execution times are given in the following table 2.1.

Table 2.1: Instruction Pipeline

Stages	stage1	stage2	stage3	stage4	stage5
Execution Time	x	2x	2x	x	2x

Let ***s*** be the number of stages. Assume all the instructions execute as above order and no branching instructions.

i. What is the clock period ***t*** in term of ***s***?

[4 Marks]

ii. What is the CPI of the above pipeline?

[4 Marks]

iii. What is the speedup of this pipeline?

[4 Marks]

Q3.

a) Briefly describe the advantages of having a hierarchical memory system.

[02 Marks]

b) Briefly describe the main modules of the hierarchical memory.

[02 Marks]

c) Consider a disk with 5400 rpm disk rotational speed, average seek time 30ms, 512-byte block size, 128-byte inter-block gap size, 20 blocks per track, 400 tracks per surface and 8 double sided disks.

i. Calculate the total capacity and useful capacity of a cylinder.

[04 Marks]

ii. If one track of data can be transferred per revolution, what is the data transfer rate?

[04 Marks]

iii. Calculate the maximum rotational delay.

[04 Marks]

iv. What is the average time to locate and transfer a single sector given its address?

[04 Marks]

Q4.

a) Briefly describe the Accumulator based computer architecture with the help of a diagram.
[04 Marks]

b) Briefly describe the fetch execute cycle with the help of a diagram.
[02 Marks]

c) Briefly describe implied, immediate, direct and indirect addressing modes.
[04 Marks]

d) Write a program using the ISA (given in the Appendix) of the Accumulator architecture of the Students' Experimental Processor (SEP) to find the Y value.

$$y = \sum_{i=1}^{5} x_i + pq$$

Assume that all elements of the array, values of p and q are stored in the memory.
[10 Marks]

Section B

Answer at least **two (2)** questions from this section.

Q5.

a) Which file allocation strategy is most appropriate for random access files? Justify your answer
[04 Marks]

b) Give a scenario where choosing a large filesystem block size might be a benefit and give and give an example where it might be an interference.
[04 Marks]

c) Draw a chart to illustrate the execution of processes listed in Table 5.1 given below for following two process scheduling methods. State all the assumptions clearly.
   a. Shortest Job First
   b. Shortest Remaining Time

Table 5.1: Execution of Processes

Arrival Time	Process	Process Time
0	P1	4
1	P2	7
2	P3	2
3	P4	2

[06 Marks]

d) Calculate average waiting time and average throughput for each scheduling method.
[06 Marks]

Q6.

a) Consider the scenario given in table 6.1 below, where "P" indicates a process and "R" indicates a resource.

Table 6.1: Scenario

Time	Action
1	P2 requests and is allocated R3
2	P4 requests and is allocated R4
3	P3 requests R4
4	P5 requests and is allocated R1
5	P1 requests and is allocated R2
6	P2 requests R2
7	P4 requests and is allocated R5
8	P1 requests R3
9	P3 requests R5
10	P4 releases R4, which is allocated to P3
11	P5 releases R1
12	P3 requests R3
13	P1 releases R2, which is allocated to P2
14	P4 releases R5, which is allocated to P3
15	P2 releases R3, which is allocated to P1
16	P2 releases R2

Use Holt's deadlocks modeling method (Resource allocation graphs) to analyze the above scenario. Show your work.

[07 Marks]

b) Is there a deadlock in the system above? Describe it.

[05 Marks]

c) Briefly explain the four conditions need to be checked for a possible deadlock by giving an appropriate example for each.

[08 Marks]

Q7.

a) Briefly explain the steps involved in handling a page fault.

[04 Marks]

b) Memory paging is a feature that permits extending the address space far beyond the available memory. [X] and [Y] denote different addresses. Name the components given as [X], [Y] and [Z] in the following diagram (Figure 7.1) and describe how the extension of the address space happens.

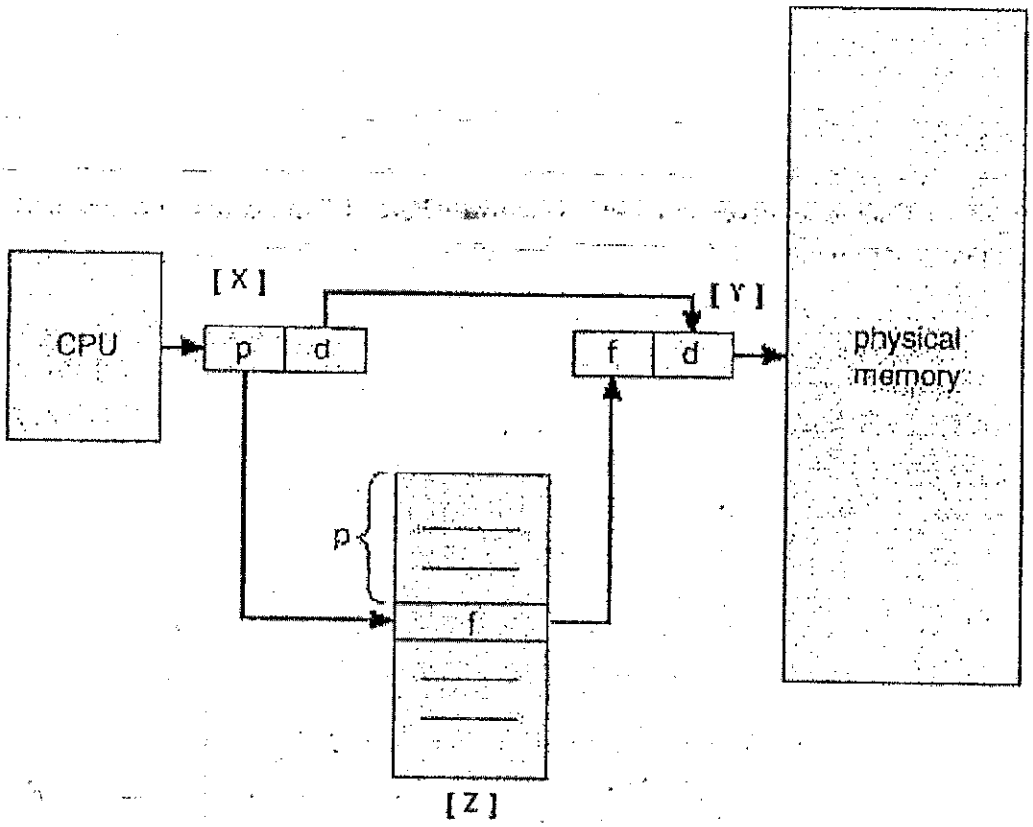

Figure 7.1: Memory Paging

[06 Marks]

c) Page size is one of the parameters of a virtual memory. Briefly describe one advantage and one disadvantage of choosing a large page size rather than a small one.

[04 Marks]

d) The following diagram (Figure 7.2) depicts CPU utilization vs degree of multiprogramming. Focus on the regions shown by (A) and B) and describe the reasons for such a behavior)

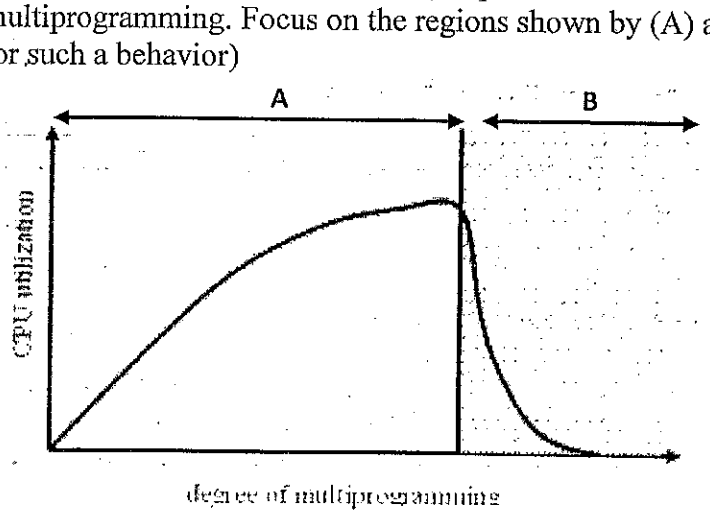

Figure 7.2: CPU Utilization vs Degree of multiprogramming

[06 Marks]

Q8.

Memory requirements for a series of processes are given in table 8.1 below. Available memory is 2MB. Processes will be requested in the sequence of P1,P2,P3,.....P7.

Table 8.1: Memory Requirements

Process No.	Memory Requirement(kB)
P1	150
P2	60
P3	620
P4	50
P5	25
P6	650
P7	515

a) Compute internal and external fragmentation under best fit and first fit allocations for the following memory allocation schemes.
   I. Fixed Partitioning
   II. Dynamic Partitioning

[12 Marks]

b) Decide which memory placement strategy is suitable to serve the above requirement. Draw suitable diagrams to justify your answer. You are expected to write down the assumption you make.

[08 Marks]

Appendix

ISA of Accumulator Architecture

Arithmetic instructions		
ADD	Addition,	Acc ← Acc. + op
SUB	Subtraction	Acc ← Acc - op
MUL	Signed multiplication	Acc (16 bit) ← Acc(8 LSBs) * op(8 LSBs)
DIV	Unsigned division	Acc ← Acc / op2
INC	Increment by 1	Acc ← Acc + 1
Logical instructions		
AND	Bit-wise And	Acc ← Acc AND op
OR	Bit-wise OR	Acc ← Acc OR op
XOR	Bit-wise XOR	Acc ← Acc XOR op
SHL	Shift left by 1-bit	CF ← Acc (MSB), op← Acc (14 down to 0) & 0
SHR	Shift right by 1-bit	CF ← Acc (LSB), Acc ← 0 & Acc (15 down to 1)
ROL	rotate left by 1-bit	CF ← Acc (MSB), op← Acc (14 down to 0) & CF
ROR	rotate right by 1-bit	CF ← Acc (LSB), Acc ← CF & Acc (15 down to 1)
NOT	One's compliment negation	op1 ← NOT Acc
Control Transfer instructions		
Conditional Branches		
JC	Jump if carry	If CF =1 then IP ← IP + Operand
JOF	Jump if over-flow	If OF =1 then IP ← IP + Operand
JS	Jump if Sign	If SF =1 then IP ← IP + Operand
JP	Jump if parity	If PF =1 then IP ← IP + Operand
JZ	Jump if result is zero	If ZF =1 then IP ← IP + Operand
Unconditional branches		
JUMP	Jump	IP ← IP + Operand
Loops		
LOOZ	Loop until zero	Count ← Count – 1 IF Count =0; Loop termination ELSE; IP ← IP + operand
Calls and Returns		
CALL	Procedure call	implied return address ← IP IP ← Immediate address
RETURN	Return from procedure	IP ← Contents of implied return address
Miscellaneous instructions		
NOP	No operation	
Data Movement instructions		
LOADacc	Copy the operand to the accumulator	Immediate: Acc ← op Direct: Acc ← memory (op)
STOREacc	Copies the accumulator to the memory address	Direct: Memory (op) ← Acc Indirect : Memory {memory (op)} ← Acc