The Open University of Sri Lanka
Department of Electrical and Computer Engineering
Final Examination –2005
ECX 3230 – Electronics **(Closed Book)**

Time: 0930-1230hrs. Date: 04.05.2006

Answer any five questions.

1. (a) Sketch the $I_D - V_{DS}$ characteristics for an n-channel JFET and indicate the regions of operation. Give expressions for the drain current in each of these regions.

(b) A JFET amplifier is shown in Figure-Q1.

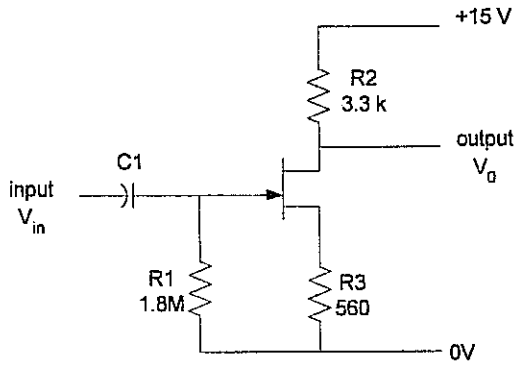

Figure - Q1

(i) Identify the component used to stabilize the bias point of the amplifier. Briefly explain how it stabilizes the bias point.

(ii) Calculate V_{DS}, V_{GS} and I_D at the dc operating point of the amplifier. Assume that the $I_{DSS} = 5mA$ and $V_P = -6V$.

(iii) Find the transconductance of the device under these operating conditions.

(iv) Calculate the gain of the amplifier for mid band frequencies. You may assume that the reactance of the capacitor is negligible at signal frequencies.

2. (a) Examine the circuit shown in Figure-Q2. A sine wave of frequency 100 *Hz* and having an amplitude of 10V is given to the input. Sketch the output waveform with the input on the same diagram indicating time and voltage values. Assume that the forward resistance, the reverse resistance and the cut-in voltage are 100Ω, 1M and zero respectively for the diode.

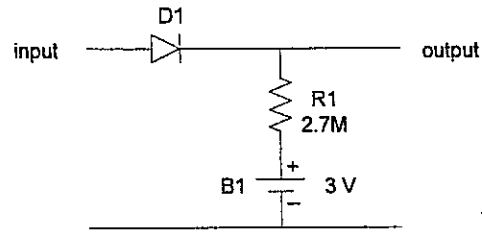

Figure-Q2

(b) Design a regulated dc power supply giving an output of 12V using a zener diode to handle load currents in the range 0-500mA. The input available is an unregulated voltage in the range 15-25V. Give the circuit diagram and calculate the values of the components selecting practical values. Assume that a minimum zener current of 20mA.
What are the main disadvantages of a basic zener regulator?

3. (a) Draw the circuit diagrams of the following.
(i) Full wave bridge rectifier with a capacitor filter.
(ii) Full wave center tap rectifier with a capacitor filter.

(b) A circuit of a dc power supply is shown in Figure-Q3.

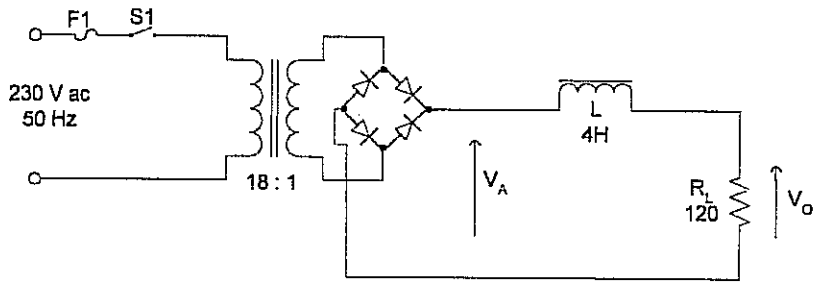

Figure-Q3

(i) Sketch the waveform of the voltage V_A indicating important voltage and time values. Assume that each rectifier diode has a nominal forward drop of 0.6V.
(ii) If it is required to have at least 10Vdc across the load, calculate the maximum winding resistance of the smoothing inductor. Also calculate the peak to peak ripple voltage across the load.

4. (a) Draw the h-parameter model for a common emitter bipolar junction transistor.
(b) A common emitter transistor amplifier is shown in Figure-Q4.

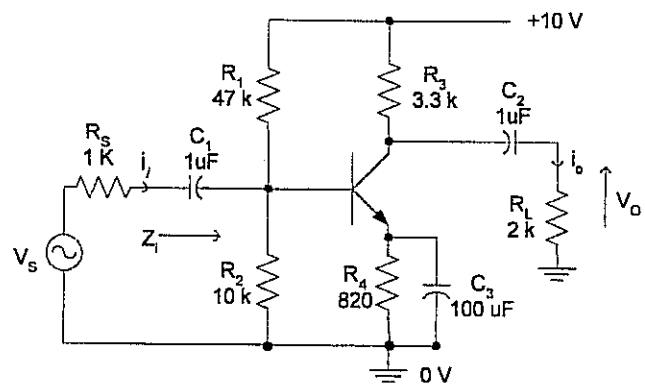

Figure-Q4

The amplifier is driven by a source having output impedance R_S of 1kΩ and the output is connected to a load R_L of 2 kΩ. The reactance of the capacitors is negligible at the signal frequencies.

(i) Draw the small signal equivalent circuit for the amplifier using h-parameters assuming h_{oe} and h_{re} are negligible.

$h_{ie} = 1.2k\Omega \qquad h_{fe} = 100$

(ii) Derive expressions for the input impedance Z_i, current gain $\frac{i_o}{i_i}$ and the voltage gain $\frac{V_o}{V_S}$ using (i) above. Also calculate the values of these.

5. A high frequency power driver circuit is shown in Figure-Q5(a). The input signal f_i fed into the analog switch is a sine wave of 250Hz. The switch is controlled by a control signal f_S. When f_S is +5V, the switch closes and the input is passed to the power amplifier of gain K. When f_S is zero, the switch opens and the input to the amplifier is zero. The relationship between f_i and f_S is shown in Figure-Q5(b).

(i) Sketch the waveform of the output V_O to a common time scale with f_i and f_S.

(ii) Derive expressions for the average value and the rms value of V_O.

You may use, $\sin^2\theta = \frac{[1-\cos 2\theta]}{2}$.

(iii) If f_i is 10sinωt and the δ is ranging from 0.4-2.0ms, calculate the range of V_O(average) and V_O(rms). Assume that the $K = 20$.

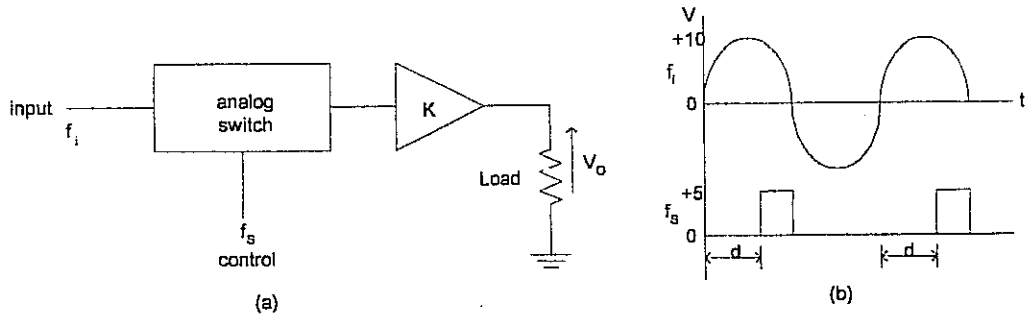

Figure-Q5

6. (a) Draw the truth table for the circuit shown in Figure-Q6(a).

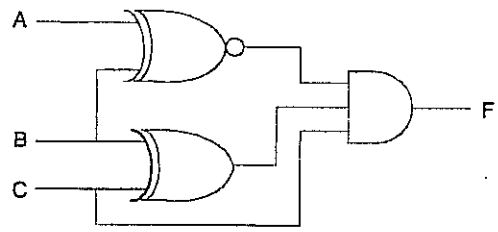

Figure-Q6(a)

(b) The inputs A and B of the circuit shown in Figure-Q6(b) are given the signals shown in Figure-Q6(c).

(i) Draw the timing diagram of the waveforms at A, B, C, D, E and F. Assume that at the initial state E = 0 and F = 1.

(ii) Draw the truth table for A, B, E and F. Hence identify the operation of the circuit.

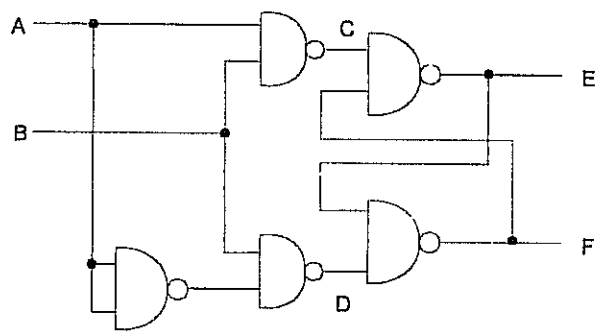

Figure-Q6(b)

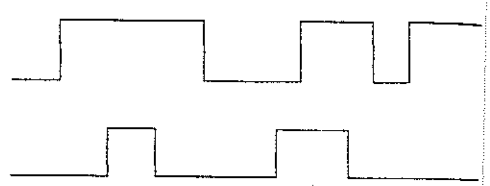

Figure-Q6(c)

7. (a) Draw the truth table for a half adder which will add two single bit numbers A and B. Give the outputs in the minimized form and implement it with minimum number of gates. Give a circuit that implements a full adder function of A and B based on half adders.

(b) Design a circuit that performs comparison between two 2-bit binary numbers A and B. The circuit must have three outputs P, Q and R, which produces P=1, Q=1 and R=1 when A>B, A=B and A<B respectively. Implement the circuit in minimized form with NAND gates.

(c) Minimize the following function using Karnaugh's map.

$F = \Sigma\, 0,1,2,5,7,8,10,14,15$

8. Consider the circuit shown in Figure-Q8.

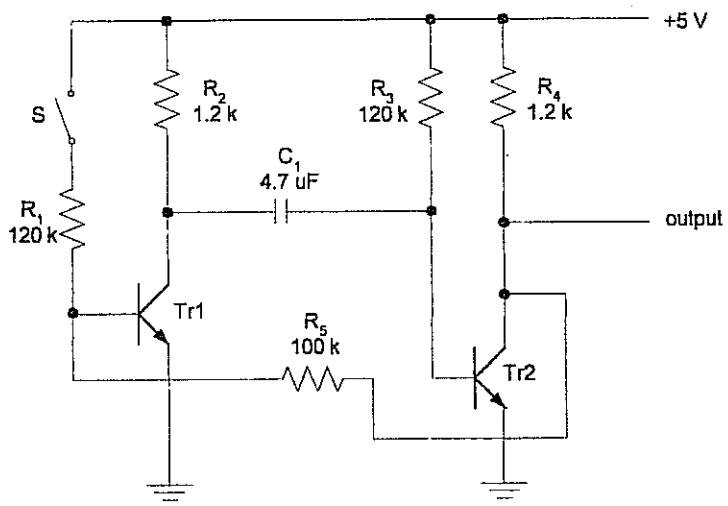

Figure -Q8

(a) Calculate the voltages at the base and collector of each transistor when the switch S is open for a long time.

(b) Assuming the condition in (a) as the initial condition, derive an expression for the base voltage of Tr2 when the switch is pressed and held. Sketch this function with the output voltage on the same axes marking voltage and time values. You may assume that the transistors are ideal.

(c) What is the purpose of R_5? State the behavior of the circuit without R_5.