The Open University of Sri Lanka
Department of Electrical and Computer Engineering
Final Examination –2009
ECX 5330 – Electronic Systems **(Closed Book)**

Time: 1400-1700hrs. Date: 03.04.2010

Answer any five questions.

1. Consider the circuit shown in Figure-Q1, where I_1, I_2 and I_3 are ideal current sources. Assume the transistors are of high gain.

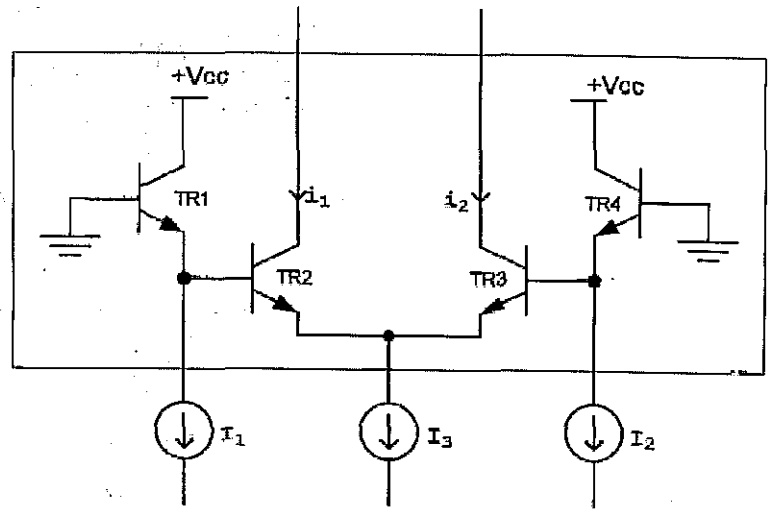


Figure - Q1

(a) Find an expression for i_o, where $i_o = i_1 - i_2$. Then evaluate it if $I_1 = (I_R + A_C \cos \omega_C t)$, $I_2 = (I_R - A_C \cos \omega_C t)$ and $I_3 = (I_S - A_m \cos \omega_m t)$.

(b) Show that it is possible to combine two of the outlined blocks with modified inputs to obtain an output signal current which is given by $K\cos(\omega_C + \omega_m)t + K\cos(\omega_C - \omega_m)t$ where K is a constant. Assume $\omega_C > \omega_m$.

(c) What is the minimum value of dc currents I_R and I_S, in terms of other variables for which the circuit can operate as expected? Hence find the value of K.

2. A multistage amplifier is shown in Figure Q2. The first stage ST1 is a transresistance amplifier having open loop gain A_R. The following stage ST2 is a transconductance amplifier having open loop gain A_G. Input and output impedance of the amplifiers are R_1, R_2, R_3 and R_4, while the input signal source is represented with I_S and R_S.

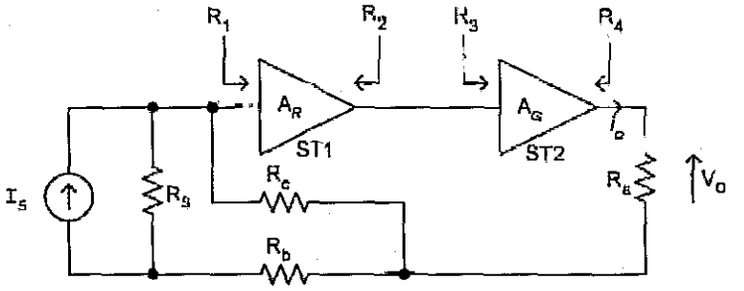


Figure-Q2

(a) Draw the open loop ac equivalent circuit considering the loading effect of the feedback network (A-circuit).

(b) Find expressions for the open loop gain in (a) and for the feedback factor of the closed loop amplifier.

(c) For the following values, calculate the open loop current gain and the feedback factor. Then calculate the current gain, input impedance and output impedance for the closed loop case.

$A_R = -100\frac{V}{A}$ $A_G = 50\frac{A}{V}$ $R_1 = 1.2k$ $R_2 = 500\Omega$

$R_3 = 1.2k$ $R_4 = 22k$ $Ra = 1k$ $Rb = 330\Omega$

$Rc = 4.7k$ $Rs = 2k$

(d) If the open loop amplifier is having a dominant pole and a gain-bandwidth product of 5×10^4 Hz, calculate the bandwidth of the closed loop amplifier.

3. The integrated circuit amplifier shown in Figure-Q3, is having a gain transfer function $-\frac{10^4}{\left(1+\frac{s}{10^5}\right)\left(1+\frac{s}{10^7}\right)\left(1+\frac{s}{10^8}\right)}$.

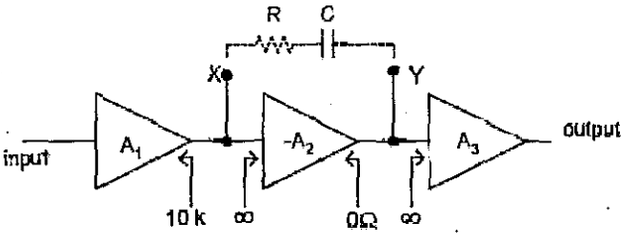


Figure-Q3

(a) Sketch the magnitude and phase Bode diagrams of the gain transfer function in the frequency range 10^2 to 10^9 rad.s^{-1}. Indicate the important slopes and the magnitude/phase values in the diagrams. You may use the log graph provided in the last page of the question paper with the scales $1" = 40$dB and $1" = 90^0$.

(b) Find the gain and phase margin when this amplifier is provided with negative feedback having a feedback factor of 0.0143. Comment on the performance in this case.

(c) An amplifier of 20dB gain is implemented using the above integrated circuit. Calculate the values of C and R of the network shown, which will provide a phase margin of 45^0. Find the feedback factor and the overall bandwidth, assuming $A_2 = 1000$. You may use pole-zero approach.

4. An infinite gain inverting high pass filter circuit is shown in Figure-Q4. You may assume that the operational amplifier is ideal.

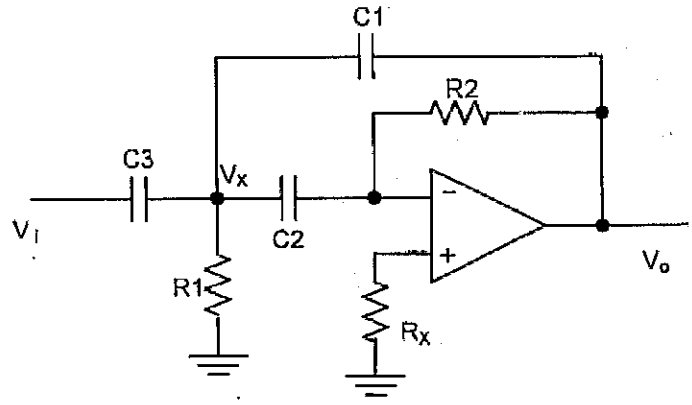


Figure - Q4

(a) Derive the voltage transfer function H(s) for this circuit.

(b) It is required to design a second order Chebyshev high pass filter with 0.5dB of pass band ripple using the above circuit. The cutoff frequency of the filter is 20kHz. Derive the component values using the transfer function obtained in (a) while showing frequency and impedance scaling clearly. You are required to use the standard low pass filter function $\frac{H_0\omega_0^2}{s^2+\alpha\omega_0 s+\omega_0^2}$ with the frequency normalized Chebyshev polynomial for 0.5dB pass band ripple $s^2+1.4256s+1.5162$. Assume that the values of $C1 = C2 = C3$.

5. Consider the BJT amplifier shown in Figure-Q5.

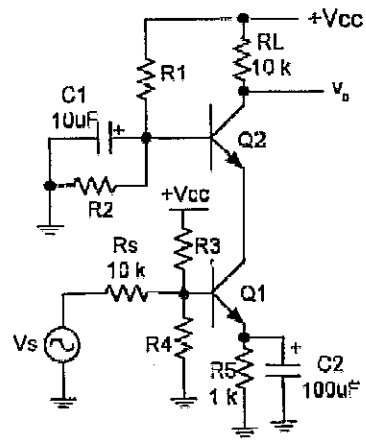


Figure - Q5

The driving source is denoted by V_s with R_s. You may neglect the effect of the biasing resistors. The data of the transistors for hybrid-π model are as follows.

$g_m = 20\frac{mA}{V}$ $\quad r_{b'e} = 5k$ $\quad r_{bb'} = 0$ $\quad r_{ce} = \infty$

$c_{b'e} = 2pF$ $\quad c_{b'c} = 2pF$

(a) Draw the high frequency equivalent circuit.

(b) Derive the multi pole voltage gain transfer function at high frequencies.

(c) Calculate the mid band gain and the pole frequencies. Hence determine the upper 3dB cut off frequency.

6. (a) Draw the circuit of a 4-bit voltage output DAC using R-2R resistive ladder. Derive an equation for the output voltage in terms of the binary inputs.

(b) Show the design and implementation of a 2-bit flash ADC indicating the design steps clearly.

(c) A temperature monitoring system using a thermocouple needs to have $\pm 0.2\ ^0C$ resolution. The thermocouple used has a sensitivity of $50\ \frac{\mu V}{^0C}$ and the range of measurement is from $0\ ^0C$ to $100\ ^0C$. This system is implemented using an op-amp and an ADC with an input voltage range of 2.5V.

(i) Calculate the number of bits required for the ADC and select a practical value.

(ii) Calculate the resolution with the selection in (a).

(iii) Show how the system is implemented and state the necessary circuit parameters. You must indicate the important points regarding the use of the op-amp in order to get the maximum accuracy.

7. (a) Explain the terms 'static hazards' and the 'dynamic hazards' in a logic circuit.

(b) Consider the logic circuit shown in Figure-Q7.

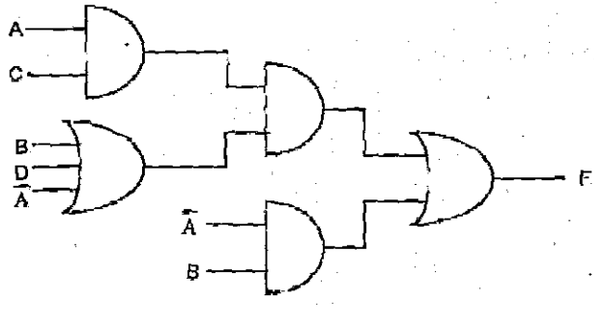


Figure-Q7

(i) Analyze this circuit and find out all static hazards. Show the input state of the variables that must exist for these hazards to happen. Hence modify the circuit to eliminate these hazards.

(ii) Implement the logic function in (b) with NAND gates ensuring hazard free operation.

8. (a) The state diagram of a shift register performing left shift is shown in Figure-Q8. Complete this state diagram indicating the states, corresponding inputs and the direction of transition.

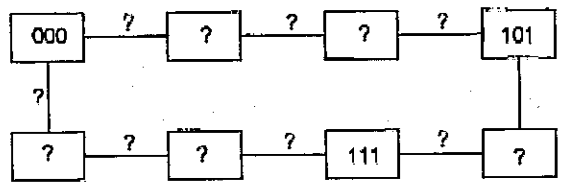


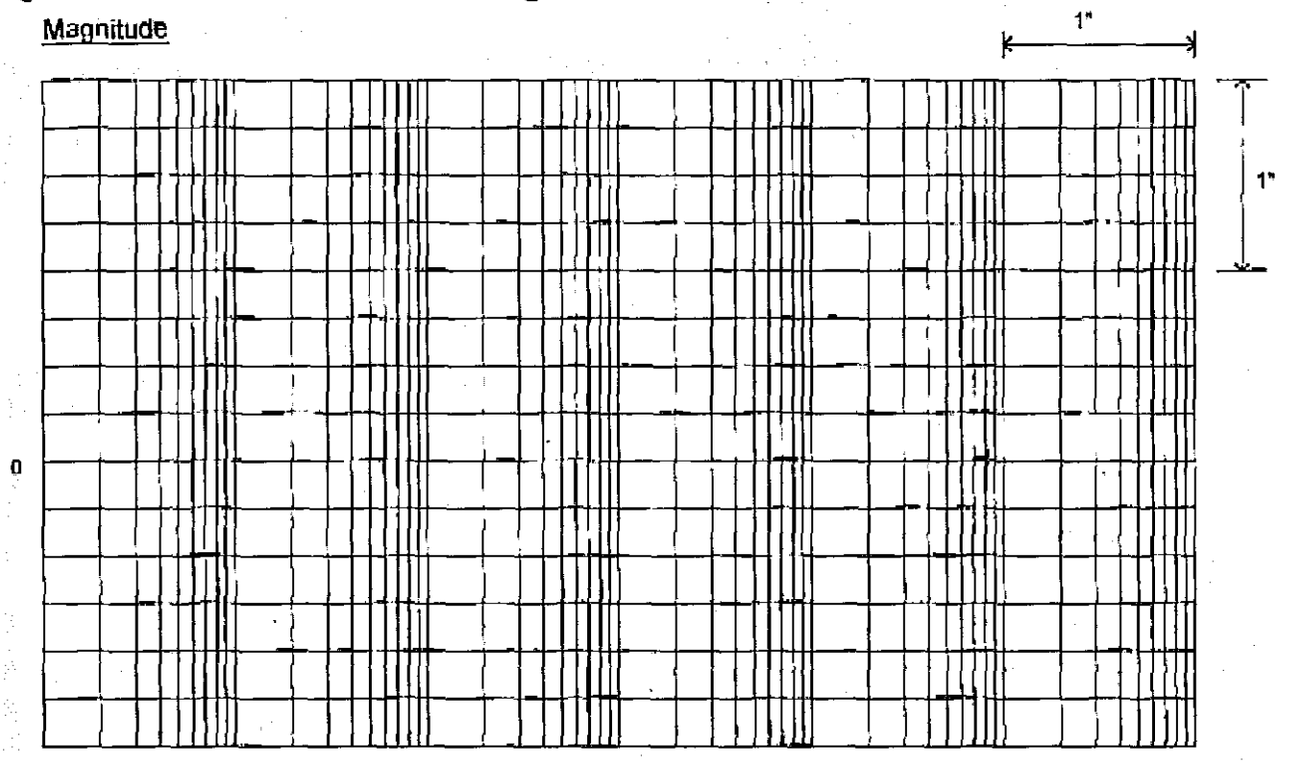
Figure-Q8

(b) Design a synchronous counter which follows the state sequence shown in (a), using a shift register and with basic gates as necessary. Show the steps of your design clearly.

(c) Implement a sequence generator to generate the binary sequence 10011010 using the counter designed in (b) with a multiplexer.

Question: 3 Reg. No:

Magnitude



Phase