THE OPEN UNIVERSITY OF SRI LANKA
DEPARTMENT OF COMPUTER SCIENCE
B. SC. DEGREE PROGRAMME 2017/2018
FINAL EXAMINATION
CPU3141: DIGITAL COMPUTER FUNDAMENTALS
CSU5306: DIGITAL ELECTRONICS
DURATION: TWO HOURS (2 HOURS)

Date: 06.10.2018 **Time: 1.30 pm – 3.30 pm**

Answer Four (04) Questions

Q1.

(i) Solve the following using binary arithmetic and represent the answers in decimal. (Cleary Show the steps)

a) 128 + 58

b) 31.510 + 33.6510

c) 3F16 / 616

d) 1011012 * 1001112

(ii) Using the ASCII Character Table given in the Annex 1, write the binary code for the following statement.

"What is the bigger value between 32 and 57?"

(iii) Simplify the following Boolean Expression using Boolean algebraic rules. Justify your simplification.

A' (A + B) + (B + AA) (A + B')

(iv) **(A+B+C+D') (A+B+C'+D) (A+B'+C+D')(A+B'+C'+D) (A'+B'+C'+D) (A'+B+C+D') (A'+B+C'+D) = F**

a) Draw the K'Map for the above PoS Boolean equation for F.

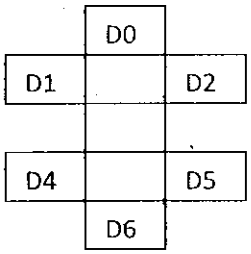
b) Minimize the K'Map and provide the answer in SoP form.

Q2.

(i) List three (03) functions of Combinational Logic Circuits and briefly describe them.

(ii) Draw AND-OR Logic circuit for the binary Full Adder. Minimize the adder circuit using XOR gates.

(iii)Binary Seven Segment Encoder is as follows.



a) Using BCD (8421) code, draw a table to display Decimal Digits in a Binary 7 Segment Encoder.

b) Using the table drawn in (a) determine the relationship between each BCD bit and decimal digits

c) Draw the related logic circuit to encode each decimal digit to BCD code.

(iv)

a) Draw the logic diagram of the 4 Input Multiplexer.

b) Draw the Block Diagram for the 4 input multiplexer.

c) Using the block diagram in (b) design a 16 X 1 Multiplexer.

Q3.

(i) Briefly describe the Set(ting) and Clear(ing) of the Flip Flops.

(ii) Realize a D – Flip Flop using a SR – Flip Flop.

(iii) Draw a block diagram of 4 bit Universal Shift Register and Describe the Write/Read functions of 1001 into the register.

(iv) Design an Asynchronous Decade Counter and a Synchronous Decade Counter.

Q4.

(i) Compare the properties of Synchronous Sequential circuits and Asynchronous Sequential Circuits. (Give 05 points).

(ii) Using the following State Table, draw the asynchronous sequential circuit. Clearly display the steps.

Present State		Next State			
		X = 0		X = 1	
0	0	0	0	0	1
0	1	1	1	0	1
1	0	0	0	1	0
1	1	1	1	1	0

(iii) **Y = (x1x2) + (x1'x3)**

a) Draw the logic circuit for the following Boolean equation for Y.

b) Does the circuit in (a) contain any hazards? (Prove your answer)

c) If Yes, derive the hazard free circuit. (Cleary display the steps)

(iv) Explain how we can avoid static hazards in sequential circuits using SR Latches?

Q5.

(i) Briefly explain how the CPU execute program instructions. (Use a block diagram).

(ii) Peripheral Modules are accessed and controlled by the software. How does the address allocation happen for the peripheral modules?

(iii) Draw a 1 bit RAM Cell using a D Flip Flop. By using this 1 bit memory cell design an 8x1 bit memory.

(iv) Explain the following Read/Write Policies.

a) Write Through with Write Allocate

b) Write Back with No Write Allocate

c) No Read Through

Q6.

(i) List four (04) types of ROM development techniques and briefly describe them.

(ii) What are the three (03) PLDs for PROMs? Draw Block Diagrams.

(iii) Using the following Programming Table, draw the Fuse Map of the relevant PLA.

	Product Term	Inputs			Outputs		
		A	B	C	F1	F2	F3
AB	1	1	1	-	1	-	1
AC'	2	1	-	0	1	1	-
B'C	3	-	0	1	-	1	1
AB'C'	4	1	0	0	1	-	1

(iv) Briefly describe the evolution of the IC (Integrated Circuit).

Annex 1

00	NUL	10	DLE	20	SP	30	0	40	@	50	P	60	`
01	SOH	11	DC1	21	!	31	1	41	A	51	Q	61	a
02	STX	12	DC2	22	"	32	2	42	B	52	R	62	b
03	ETX	13	DC3	23	#	33	3	43	C	53	S	63	c
04	EOT	14	DC4	24	$	34	4	44	D	54	T	64	d
05	ENQ	15	NAK	25	%	35	5	45	E	55	U	65	e
06	ACK	16	SYN	26	&	36	6	46	F	56	V	66	f
07	BEL	17	ETB	27	'	37	7	47	G	57	W	67	g
08	BS	18	CAN	28	(	38	8	48	H	58	X	68	h
09	HT	19	EM	29	)	39	9	49	I	59	Y	69	i
0A	LF	1A	SUB	2A	*	3A	:	4A	J	5A	Z	6A	j
0B	VT	1B	ESC	2B	+	3B	;	4B	K	5B	[	6B	k
0C	FF	1C	FS	2C	´	3C	<	4C	L	5C	\	6C	l
0D	CR	1D	GS	2D	-	3D	=	4D	M	5D	]	6D	m
0E	SO	1E	RS	2E	.	3E	>	4E	N	5E	^	6E	n
0F	SI	1F	US	2F	/	3F	?	4F	O	5F	_	6F	o

NUL	Null	FF	Form feed	CAN	Cance
SOH	Start of heading	CR	Carriage return	EM	End of
STX	Start of text	SO	Shift out	SUB	Substi
ETX	End of text	SI	Shift in	ESC	Escape
EOT	End of transmission	DLE	Data link escape	FS	File se
ENQ	Enquiry	DC1	Device control 1	GS	Group
ACK	Acknowledge	DC2	Device control 2	RS	Record
BEL	Bell	DC3	Device control 3	US	Unit se
BS	Backspace	DC4	Device control 4	SP	Space
HT	Horizontal tab	NAK	Negative acknowledge	DEL	Delete
LF	Line feed	SYN	Synchronous idle		
VT	Vertical tab	ETB	End of transmission block		