The Open University of Sri Lanka
Department of Electrical and Computer Engineering
Diploma in Technology
ECX3230 – Electronics
Final Examination – 2011

Date:24.02.2012 Time: 0930 – 1230 hrs

Answer any five questions

1)

a) Explain the depletion layer behavior when an external battery connected across the diode. (Consider all possible biasing). [3 marks]

b) A voltage regulator circuit is shown in figure 1.1.

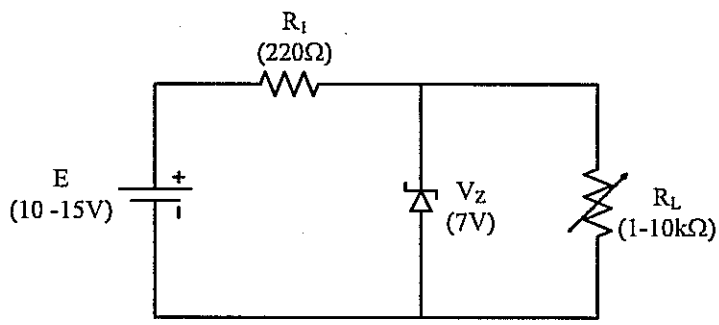

Figure 1.1

i) What is the output voltage? [1 mark]

ii) Calculate the maximum current through the Zener diode and maximum current through the load. [6 marks]

iii) Maximum power dissipation of the Zener diode. [1 mark]

c) Figure 1.2 is an equivalent circuit model of a tunnel diode.

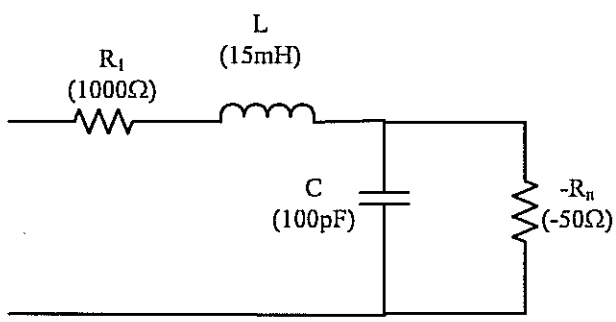

Figure 1.2

i) Derive an equivalent for the circuit oscillation. [6 marks]

ii) Calculate the frequency of oscillation. [3 marks]

2) A small signal amplifier is shown in figure 2. Current gain of the transistor is 100.

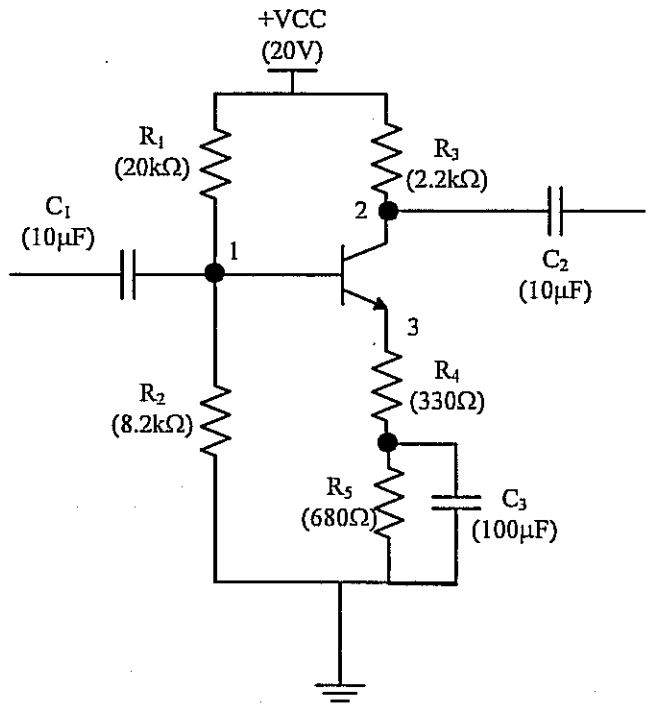

Figure 2

i) What is the configuration of this circuit? [1 mark]
ii) Calculate the Test point 1, 2 and 3 voltages of the circuit. [5 marks]
iii) Draw the DC load line. [3 marks]
iv) Write the biasing method used for the amplifier. [1 mark]
v) Derive the stability equation for this amplifier. [4 marks]
vi) Comment on the stability. [3 marks]
vii) Draw the output of the signal when 50 mV/10 KHz sinusoidal input signal is fed to the circuit. [3 marks]

3)

a) Thyristor circuit is shown in figure 3.1

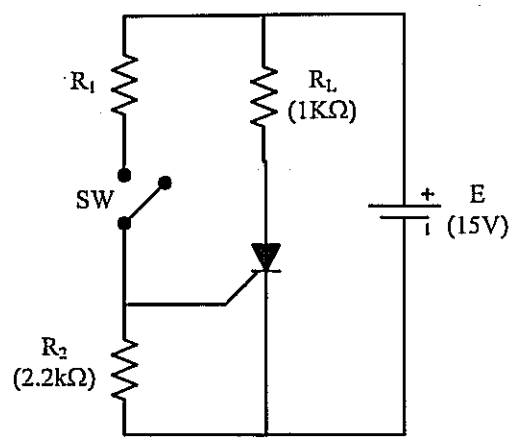

Figure 3.1

Triggering gate voltage =3V

Triggering gate current =1mA

Holding voltage =1V

i) Calculate the R1 resistor value, when the switch is closed. [3 marks]

ii) Calculate the power dissipation of the load. [2 marks]

iii) If a 12V/100Hz sinusoidal AC source is connected instead of 12V DC source. Then the switch is closed after 2ms. Draw the output signal with reference to the input signal. [4 marks]

b) A JFET amplifier shown in figure 3.2

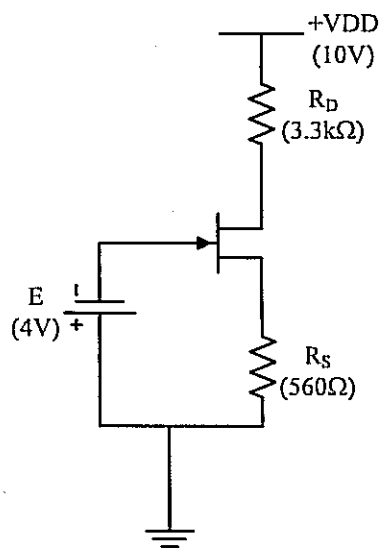

Figure 3.2

I_{DSS} =10mA

V_P = -5V

Calculate the

(i) Voltage at Gate terminal [1 mark]

(ii) Gate source voltage [8 marks]

(iii) Drain current. [2 marks]

4) A power supply unit is shown in figure 4.

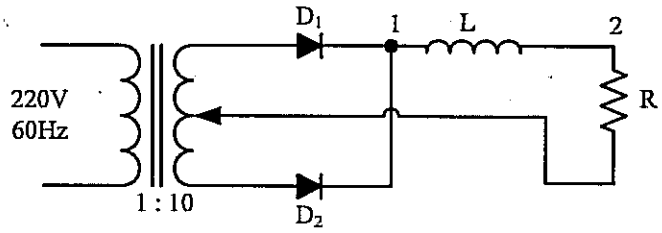

Figure 4

a) Write the type of rectification of this circuit. [2 marks]
b) Draw the signal at Test point 1 and 2 with reference to the input signal. [6 marks]
c) Derive an expression for the ripple factor of the filter given in the circuit. [6 marks]
d) Design a regulator circuit to improve the regulation of the figure 4. (Give components and values) [6 marks]

5) A two stage amplifier is shown in figure 5. h_{fe} and h_{ie} of the transistor is 1.5kΩ and 50 respectively. Neglect the effect of h_{re} and h_{oe}.

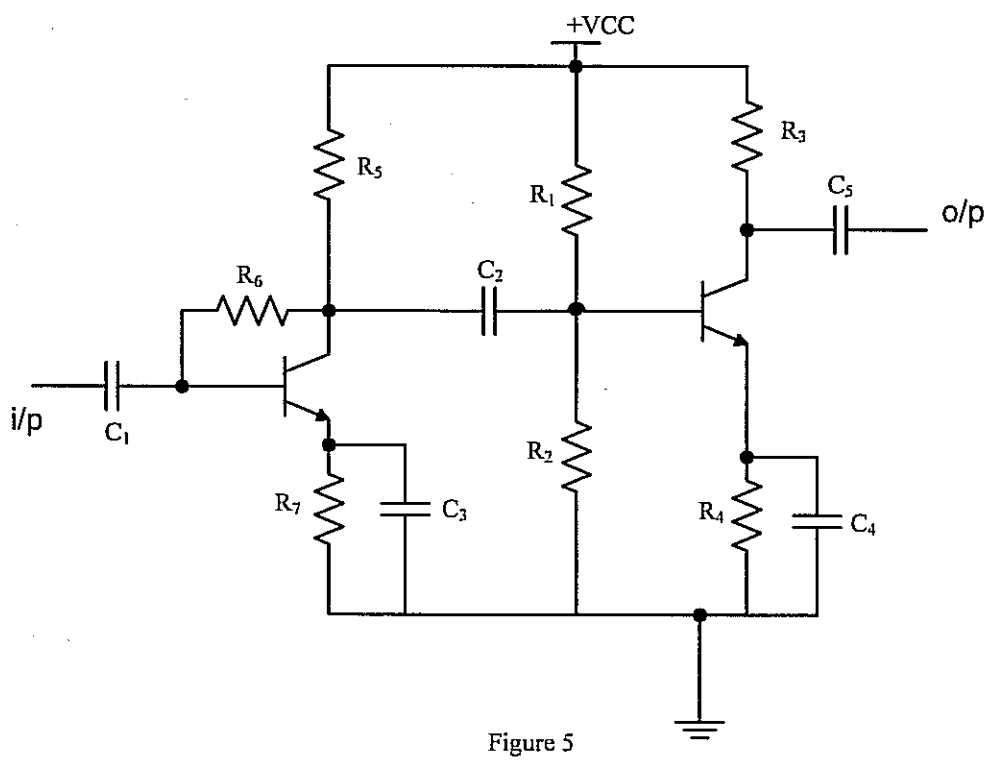

Figure 5

a) Draw an AC equivalent circuit for the figure 5. [4 marks]
b) Derive an expression for
   i) Input impedance [2 marks]
   ii) Current gain [3 marks]
   iii) Voltage gain of first stage [2 marks]

iv) Voltage gain of second stage [2 marks]

c) Hence derive the total voltage gain of the figure 5. [2 marks]

d) Draw the frequency response of the amplifier voltage gain (consider the frequency range from 1 kHz – 1 MHz). Use logarithmic scale. [5 marks]

6)

a) Convert the following

i) 1101101 binary integer to decimal [2 marks]

ii) 0.011 binary fraction to decimal [2 marks]

iii) 10001101.01011 binary numbers to hexadecimal [2 marks]

b) Write the Boolean equitation for the output of figure 6. [4 marks]

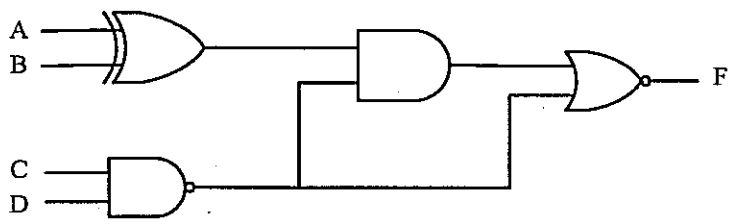

Figure 6

c) Simplify the following Boolean function using Boolean algebra. [5 marks]

$$f = \bar{A}\bar{B}\bar{C}D + \bar{A}B\bar{C}D + A\bar{B}\bar{C}D + A\bar{B}CD + A\bar{B}C\bar{D} + AB\bar{C}D + ABCD$$

d) Implement the simplified function of part c) with 3 input NOR gates. [5 marks]

7)

a) The figure 7 shows a multivibrator circuit.

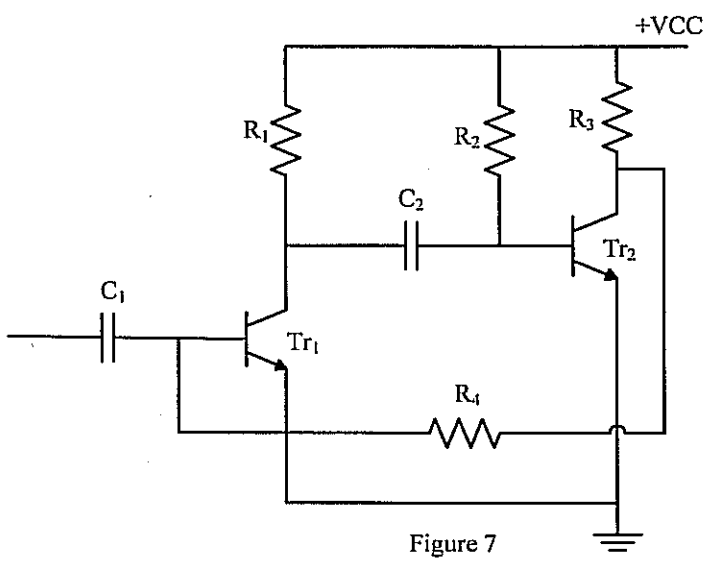

Figure 7

i) Explain the operation of this circuit. [6 marks]

ii) Draw the waveforms at the output and the base of Tr_2 with a trigger pulse of +2V.

[4 marks]

iii) Write the type of this multivibrator. [2 marks]

b) Sketch the output waveforms with respect to the input 5V/10kHz sinusoidal waveform for the following circuits. [8 marks]

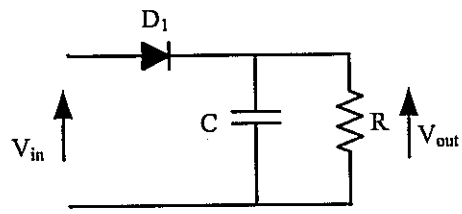

Figure 7.2

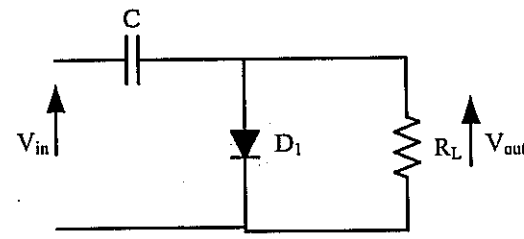

Figure 7.3

8) Design a counter circuit which counts from 1 to 7.

a) How many flip flops are required to design the counter? [1 mark]
b) Draw the state diagram for the counter. [3 marks]
c) Write the truth table? [6 marks]
d) Simplify the functions using karnaugh maps. [6 marks]
e) Design the circuit with required components. [4 marks]