The Open University of Sri Lanka
Department of Electrical and Computer Engineering
ECX3230 – Electronics
Final Examination – 2013
Date:26.07.2013 Time: 0930 – 1230 hrs

Answer Five Questions

1) A single stage amplifier circuit is shown in figure1. Silicon transistor having current gain of 50 is used for the design.

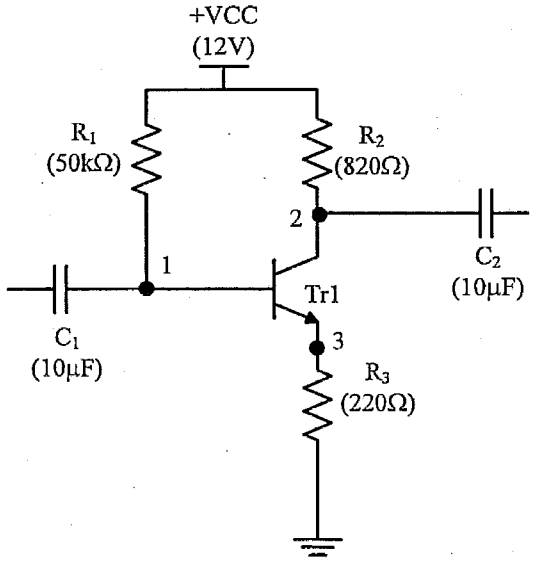

Figure 1

a) Write the configuration of the transistor amplifier. [2 marks]
b) Calculate the current through all the resistors. [6 marks]
c) Sketch the DC load line and mark all the necessary points in the graph. [5 marks]
d) Mark the Q point in the load line. [2 marks]
e) Write the biasing method used for this amplifier. [2 marks]
f) Derive and calculate the stability factor for the amplifier shown in figure 1. [4 marks]
g) Comment on the stability factor. [4 marks]

2)

a) A full wave bridge rectifier connected to the secondary side of the transformer rectifies a 10Vrms secondary voltage.
   i) If the primary winding is connected to the 220V/50Hz line, what is the turn ratio of the transformer? [3 marks]
   ii) If the rectifier has Si diodes, what is the peak output voltage of the rectifier? [2 marks]

b) A zener regulator circuit is designed with Rs =20 Ω and zener voltage of 5.6V.zener diode operates in 1mA ≤ Iz ≤ 300mA with the load current of $0 \leq I_L \leq 200$mA. Draw the circuit and calculate the range of the unregulated supply voltage. [10 marks]

c) Design a power supply circuit which regulates at 5.6 V output voltage and operates in 0 to 200 mA. Use the 2 a) and b) circuits and the knowledge of the power supply theory. [10 marks]

3)

a) Tabulate the truth table for the circuit shown in figure 3.1 [5 marks]

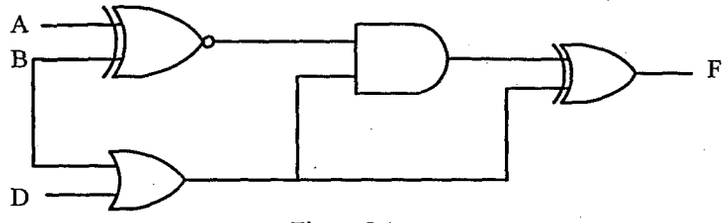

Figure 3.1

b) The input A& B of the circuit shown in figure 3.2 are given the signals shown in figure 3.3

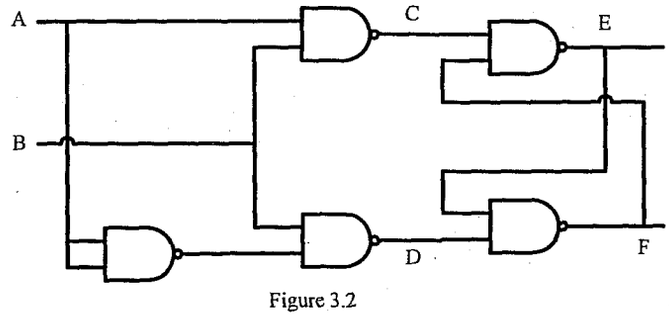

Figure 3.2

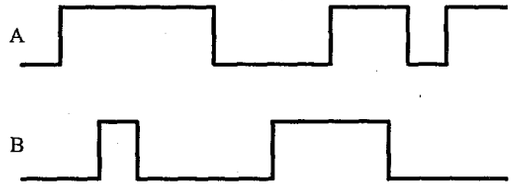

Figure 3.3

i) Draw the timing diagram of the waveforms at A, B, C, D, E and F. Assume that the initial state E = 0 and F = 1. [10 marks]

ii) Draw the truth table for A, B, E, and F. Hence identify the operation of the circuit. [10 marks]

4)

a) Minimize the following function using Karnaugh's map
$F(A,B,C,D) = \sum 0,1,2,5,7,8,10,14,15$ [6 marks]

b) A digital logic gate is represented by the figure 4.

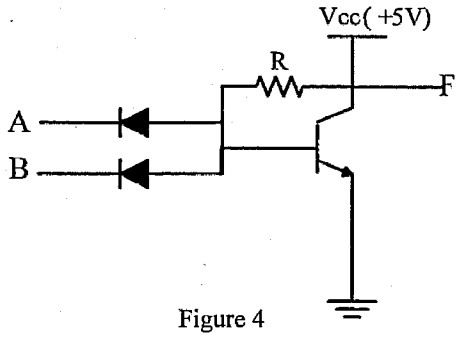

Figure 4

i) Write the truth table for the circuit shown in figure 4. [4 marks]
ii) Write the Boolean expression. [3 marks]
iii) Identify the gate. [2 marks]

c) Design a circuit that performs comparison between two 2-bit binary numbers A & B. The circuit must have three outputs P, Q & R, which produces P = 1, Q = 1 & R = 1, when A>B, A=B and A<B respectively.
i) Write the output function for P, Q and R. [3 marks]
ii) Implement the circuit in minimized form with NAND gates. [7 marks]

5)

a) Draw the h parameter model for a common emitter bipolar junction transistor.[3 marks]
b) A common emitter transistor amplifier is shown in figure 5. The amplifier is driven by a source having source impedance R_S of 1kΩ and the output is connected to a load R_L of 2.2kΩ. Neglect the reactance of the capacitors at the signal frequencies..

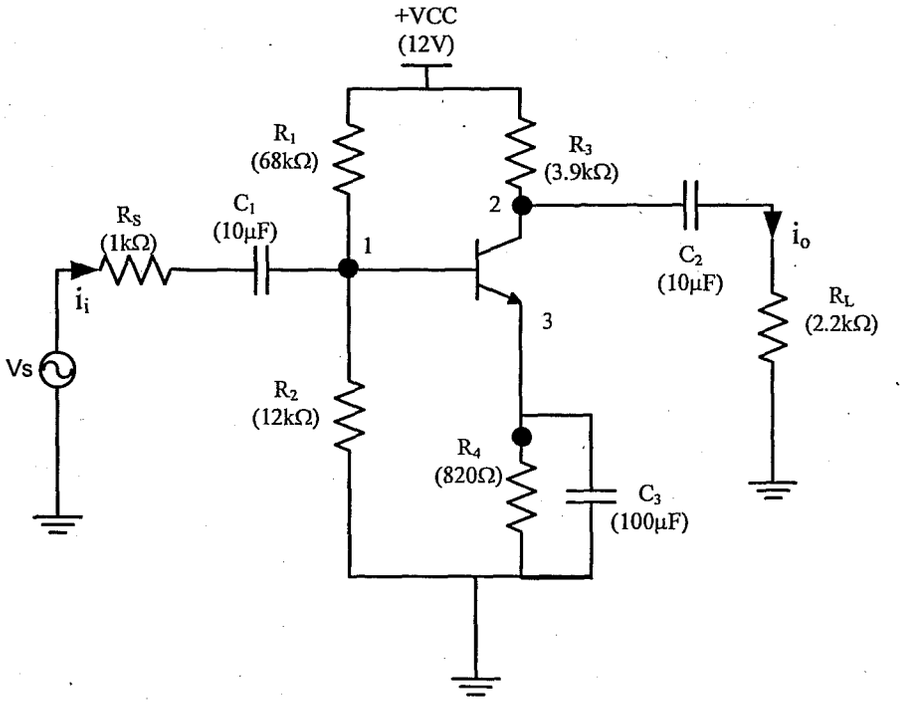

Figure 5

i) Draw the small signal equivalent circuit for the amplifier using h parameter model assuming h_{oe} and h_{re} are negligible. $h_{ie} = 1.2k\Omega$ and $h_{fe} = 100$. [7 marks]

ii) Derive expressions for the
(1) Input impedance
(2) Current gain
(3) Voltage gain [12marks]

iii) Calculate the values of the above b) ii). [3 marks]

6)

a) A sine wave of frequency 100Hz and amplitude of 10V is given as the input to the circuit shown in figure 6.1. Sketch the output waveform with the input on the same diagram indicating the time and voltage values. Explain the operation of figure 6.1. Assume diodes to be ideal. [8 marks]

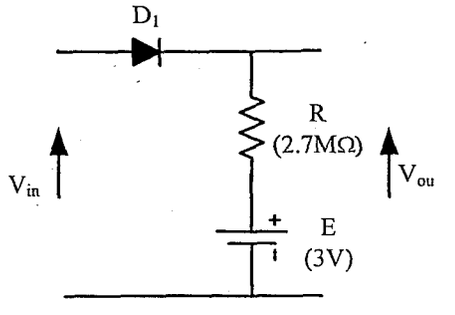

Figure 6.1

b) Design a clamper circuit to generate an output to a given input shown in figure 6.2. Explain the function. [13marks]

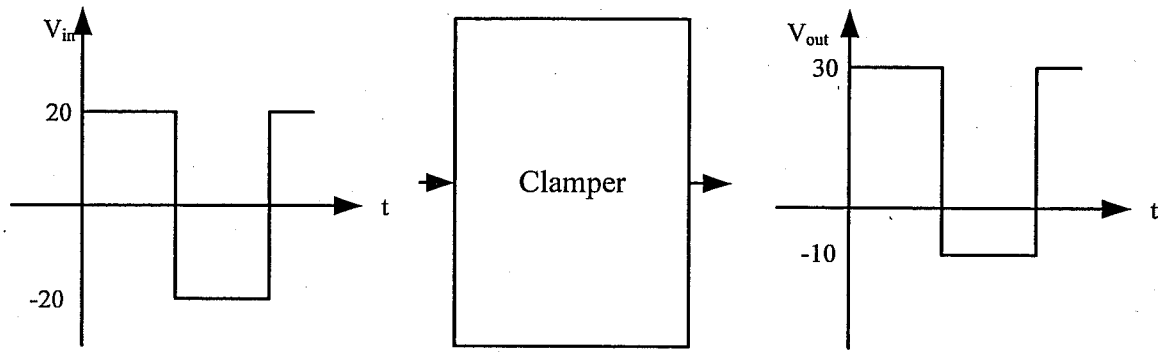

Figure 6.2

7)

a) An application of an operational amplifier is shown in figure 7.

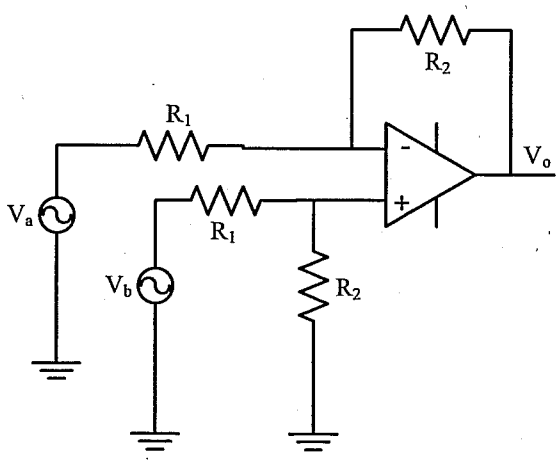

Figure 7

i) Derive an expression for the output of the circuit shown in figure 7. [8 marks]

ii) Write the operation of this circuit. [3 marks]

iii) If V_a is 5 sin1000t and V_b is 10 sin 1000t. Draw the output of the circuit with time and voltage values. Consider $R_1 = R_2 = 1k\ \Omega$ [4 marks]

b) Write short note for the following

i) UJT [5 marks]

ii) N channel JFET [5 marks]

8)

a)

i) Draw the V-I characteristics of a thyristor. [5 marks]

ii) A half wave rectifier circuit is shown in figure 8.

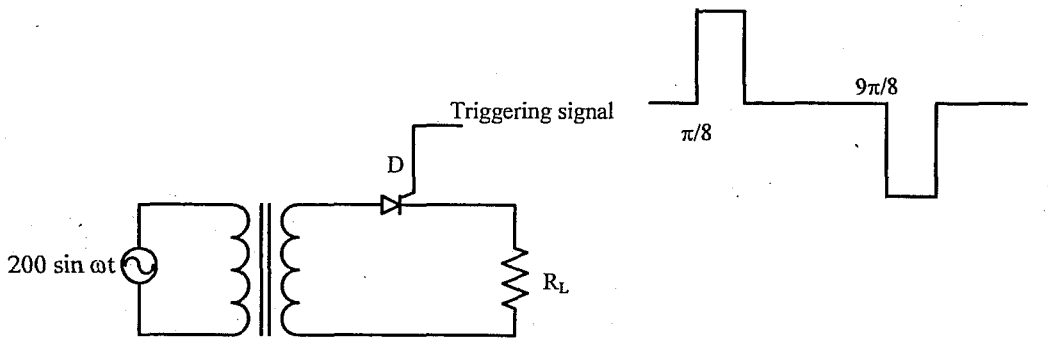

Figure 8

(1) Draw the waveform across the load. [6 marks]

(2) If the triggering signal is applied at $\pi/2$ of the signal input, what will happen to the power of the load? [4 marks]

b)

i) Draw a RLC circuit. [1 mark]

ii) The circuit current of the RLC circuit is 3mA. Voltage across inductor and the capacitor is 30V and 18V respectively. The resistance of the resistor is 1000Ω.

(1) What is the supply voltage to the RLC circuit? [3 marks]

(2) Derive an expression for the oscillation of the circuit; hence calculate the frequency of oscillation. [6 marks]