The Open University of Sri Lanka
Department of Electrical and Computer Engineering
Bachelor of Technology
ECX3230 – Electronics
Final Examinations – 2014/15 (Closed Book)

Date: 07.08.2015   Time: 09.30 – 12.30

Answer any five questions.

1.

   a. Simplify the following functions using Boolean algebra

   i. $F_1 = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,B\overline{C} + A\overline{B}\,\overline{C} + AB\overline{C}$ [2 marks]

   ii. $F_2 = \overline{A}\,B\overline{C}\,\overline{D} + \overline{A}\,B\overline{C}D + \overline{A}\,BC\overline{D} + \overline{A}\,BCD + AB\overline{C}D + ABCD$

   [2 marks]

   b. Simplify the following logic function using Karnaugh map.

   i. $f(A,B,C,D) = (1,5,9,10,11,13,14,15)$ [3 marks]

   ii. $f(A,B,C,D) = (0,1,2,5,6,7,8,9)$ [3marks]

   c. Implement the simplified logic function obtained in

   i.   (3.a.i.) using two input NAND gates.   [5 marks]

   ii. (3.a.ii) using two input NOR gates.   [5 marks]

2.

   a. Name the sections in a stabilized power supply unit and explain the function of each section.   [4 marks]

   b. Inductor - capacitor circuit is shown in figure 2. Input signal is

   $e_i = \dfrac{2E_m}{\pi} - \dfrac{4E_m}{3\pi}\cos(2\omega t)$, angular frequency (ω) is 100 Hz.
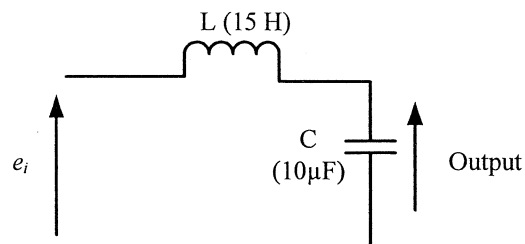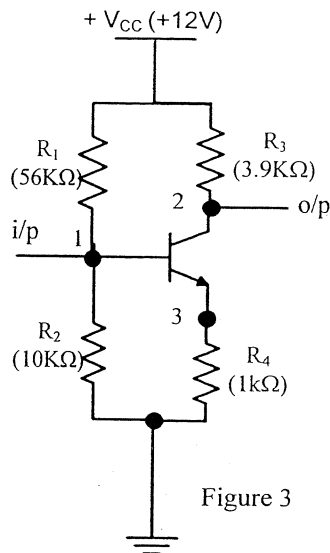

Figure 2

   i.   Derive an equation for the ripple factor of the circuit shown in figure 2.   [5marks]

   ii.   Hence calculate the ripple factor.   [2 marks]

   iii. Explain the advantage of the circuit shown in figure 3 over inductive filter.   [3marks]

c. Design a stabilizer circuit to have a 0% voltage regulation. , Output voltage maintain in 12 V with the input voltage variation of $14\pm10\%$ V.Load current must be capable of handling 0.1 to 2A range. [Note: assume a characteristics of transistor which you need for the calculation]   [6 marks]

3. A single stage transistor amplifier is given in figure 3. Si Transistor has a high current gain.

Figure 3

a. Name the configuration of the circuit shown in figure 3.   [2marks]
b. Calculate the test point voltages 1, 2, 3.   [4marks]
c. Draw the D.C load line of the amplifier. Clearly state necessary calculations.
                [4 marks]
d. According to your knowledge state the best Q point position and any modification to the amplifier design to achieve the best Q point.   [3 marks]
e. Derive an equation for the stability factor for the circuit shown in figure 5.
                [5 marks]
f. Hence calculate the stability factor for the shown in figure 3.   [2 marks]

4.

a. Compare an operational amplifier with a junction field effect transistor.
                [4 marks]
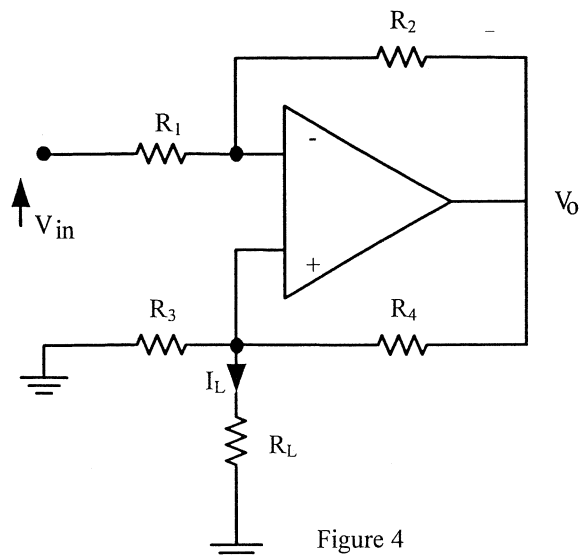b. An operation amplifier circuit shown in figure 4.

Figure 4

i. Derive a function relating V_{in}, V_o and I_L. [6 marks]

ii. Name the operation of the circuit in figure 4, using the derived function in 4.b.i [3 marks]

iii. If $\dfrac{R_1}{R_2} = \dfrac{R_3}{R_4}$., show that the load current (I_L) is proportional to input voltage (V_{in}). [4 marks]

iv. Calculate the output signal, if the $V_{in}= 2$ V , $\dfrac{R_1}{R_2} = \dfrac{1}{2}$ and R1 =1kΩ [3 marks]

5.

a. Tabulate the similarities and differences in Thyristor and a Triac. [4 marks]

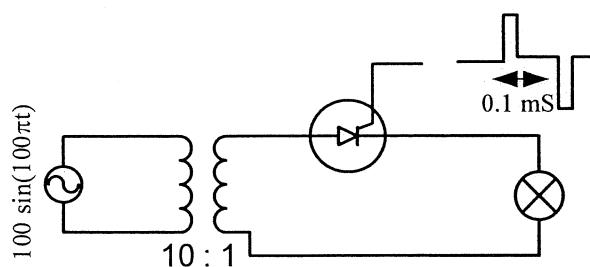b. The power delivered to a load is controlled by a Thyristor. Figure 5 shows the thyristor circuit.

Figure 5

i. Explain the operation of the circuit shown in figure 5. [3 marks]

ii. Sketch the waveform across the load with reference to the AC source signal. [3marks]

iii. Calculate the power delivered to the load? [4marks]

iv. Comment on the delivered power to the load, if the thyristor is replaced with a triac. [6 marks]

6.

   a.   Show how you use a JK flip flop to form a D flip flop and give its truth table.

                                                                                      [4marks]

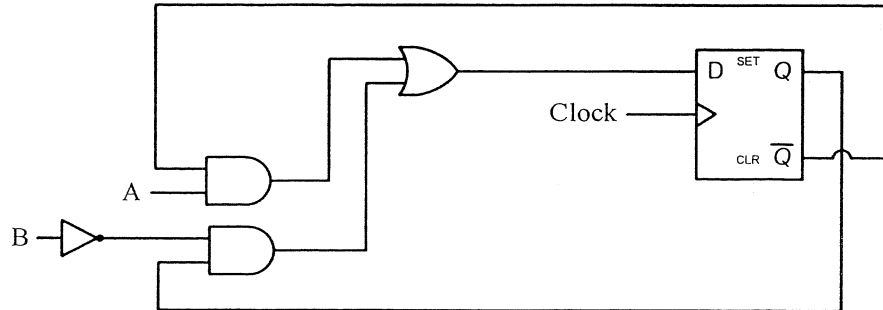   b.   Figure 6 shows a circuit forms of a D flip flop and combinational logic gates.

Figure 6

        i.   Derive truth table for this circuit (figure 6)   [8 marks]

       ii.   Identify the operation.   [8 marks]

7.

   a.   Write down the advantages of Field effect transistors over bipolar transistors.

                                                                                     [4 marks]

   b.   Consider the circuit shown in figure 7. I_{DSS} and pinch off voltage of the JFET is 12mA and -3V respectively.
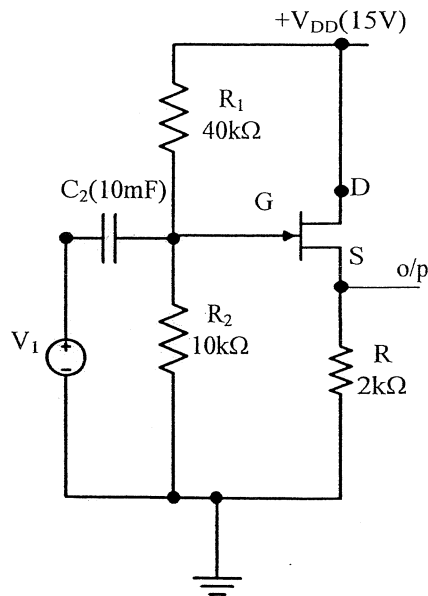

Figure 7

        i.   What is the amplifier configuration used in this circuit?   [2 marks]

       ii.   Find the gate source voltage, when no input signal is applied.

                                                                         [6 marks]

      iii.   Hence find the Drain current of the channel.   [4 marks]

iv.   Draw the ac equivalent circuit for the figure 7 and derive the voltage gain of the circuit.   [4 marks]

8.

a.   Write an application for the three configurations of an amplifier.   [3 marks]
b.   A two stage transistor amplifier circuit is shown in figure 8. Input impedance and forward current gain of the transistors are 5kΩ and 50. h_{oe} and h_{re} are negligible.
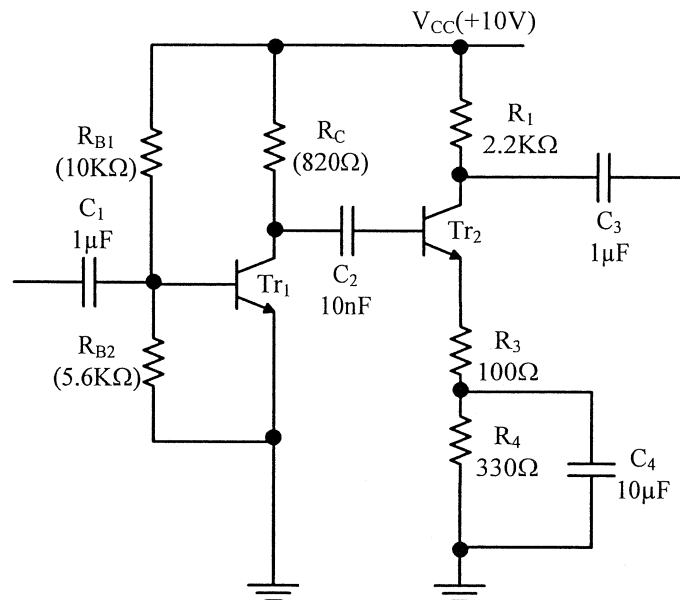

Figure 8

c.   Draw the h parameter model for amplifier circuit shown in figure 8. [5 marks]
d.   Using the circuit obtain in 8.c, derive an expressions for voltage gain, current gain and input impedance.   [9 marks]
e.   Hence calculate the voltage gain, current gain and input impedance. [3 marks]