The Open University of Sri Lanka
Department of Electrical and Computer Engineering
ECX4150 –Electronics II
Final Examination – 2014/2015

Date: 2015-08-07 Time: 0930-1230

This paper has two sections. Answer five questions selecting at least one question from Section B.
Adhere to the usual notations.

Section A

Q1.

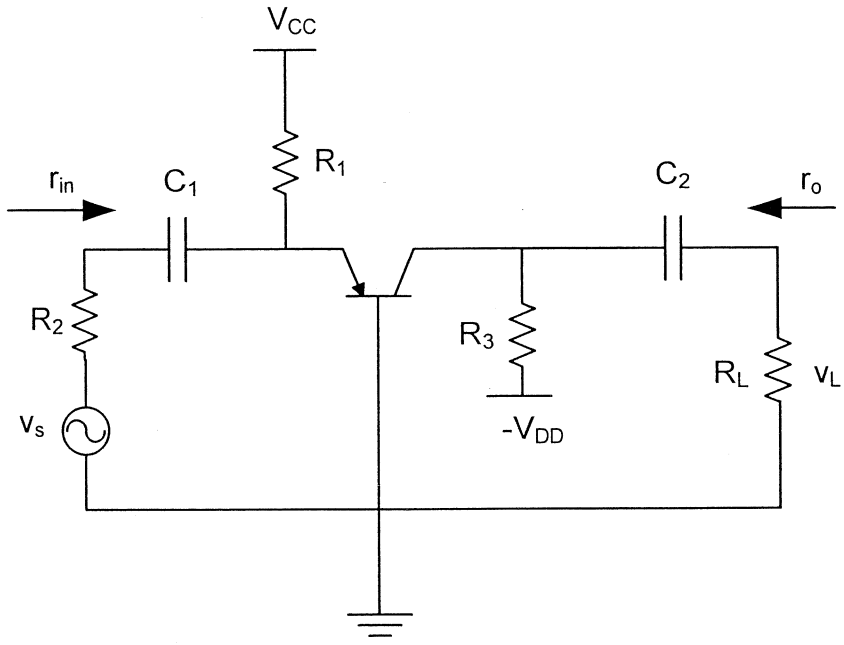


Figure –Q1

Let,

$h_{ib} = 15\Omega$ $R_1 = 1k\Omega$ $V_{CC} = 10V$ $-V_{DD} = -15V$

$R_2 = 50\Omega$ $h_{fb} = -0.992$ $R_3 = 9.1k\Omega$ $R_L = 22k\Omega$

a. Draw the h-parameter equivalent circuit of the circuit arrangement in the above Figure-Q1. (8Marks)
b. Find r_{in} and r_o. (6Marks)
c. Calculate $\frac{v_L}{v_s}$. (6Marks)

Q2.

a. Tabulate two similarities and two differences in Thyristor and a Triac. (4Marks)

b. The power delivered to a load is controlled by a Thyristor. Figure-Q2 shows a Thyristor circuit.

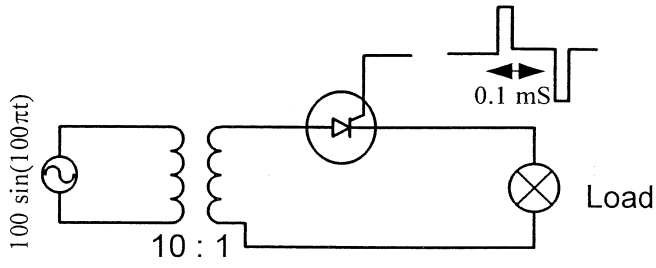


Figure –Q2

i. Explain the operation of the circuit shown in figure-Q2. (3Marks)

ii. Sketch the waveform across the load with reference to the input signal. (3Marks)

iii. Calculate the power delivered to the load? (4Marks)

iv. Comment on the delivered power to the load, if the Thyristor is replaced with a Triac. (6Marks)

Q3.

a. Show the output waveforms and conduction angles of different classes of power amplifiers. (6Marks)

b. Class B power amplifiers provide a better efficiency than Class A. Discuss a main disadvantage of Class B over Class A. Further discuss a method to overcome the above disadvantage. (5Marks)

c. A Class B push-pull power amplifier delivers $16W$ to a 8Ω load. It uses a $\pm 20V$ DC power supply. Determine,

i. Peak current drawn from each supply. (2Marks)

ii. Total power supplied to the circuit. (2Marks)

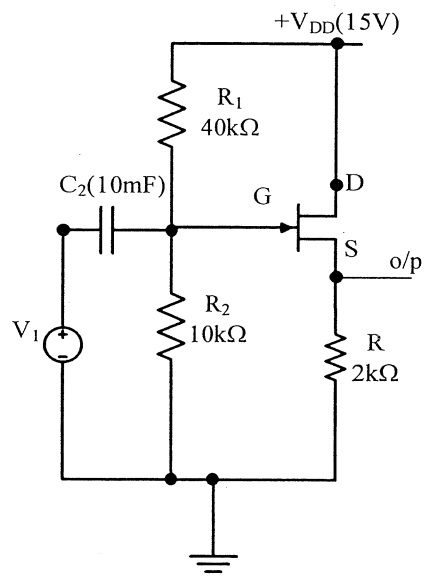
iii. Power efficiency. (2Marks)

iv. Maximum power dissipation capability for each transistor. (3Marks)

Q4.

a. List the advantages of field effect transistors over bipolar junction transistors. (4Marks)

b. Consider the circuit shown in figure-Q4. I_{DSS} and pinch off voltage of the JFET is 12mA and -3V respectively.



Figure–Q4

i. What is the amplifier configuration used in this circuit? (2Marks)

ii. Find the gate source voltage, when no input signal is applied. (6Marks)

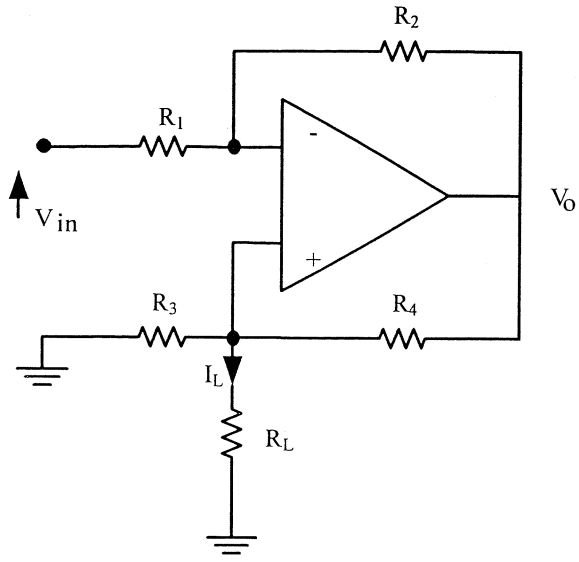
iii. Hence find the Drain current of the channel. (4Marks)

iv. Draw the ac equivalent circuit for the figure-Q4 and derive the voltage gain of the circuit. (4Marks)

Q5.

a. List three characteristics of an ideal operational amplifier. (3Marks)

b. An operation amplifier circuit shown in figure-Q5.



Figure–Q5

i. Derive a function relating V_{in} and I_L. (8Marks)

ii. Name the operation of the circuit in figure-Q5, using the derived function in 5.b.i (4Marks)

iii. If $\frac{R_1}{R_2} = \frac{R_3}{R_4}$, calculate the output signal, for V_{in}= 2 V. (5Marks)

Section B

Q6.

a. Show how you use a JK flip flop to form a D flip flop and give its truth table. [4marks]

b. Figure 6 shows a circuit forms of a D flip flop and combinational logic gates.

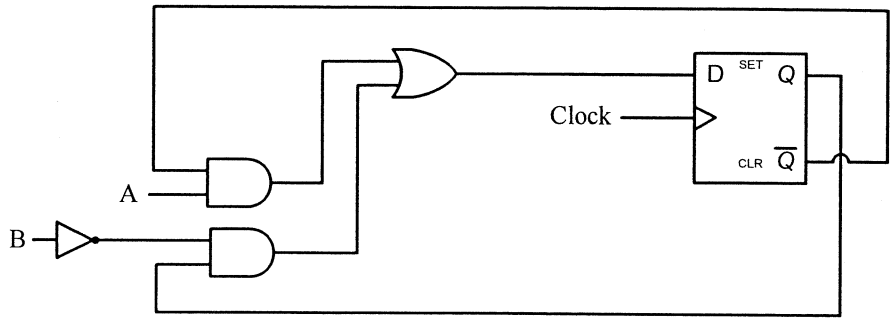


Figure 6

Derive truth table for this circuit (figure 6) and identify the operation. [6marks]

c. Draw the state diagram for the 3 bit down counter using D flip flop.
   i. Write the truth table for the design. [5marks]
   ii. Draw the circuit using flip flop and logic gates. [5marks]

Q7.

a. Simplify the following functions using Boolean algebra
   i. $F_1 = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}B\overline{C} + A\overline{B}\,\overline{C} + AB\overline{C}$ [2 marks]
   ii. $F_2 = \overline{A}B\overline{C}\,\overline{D} + \overline{A}B\overline{C}D + \overline{A}BC\overline{D} + \overline{A}BCD + AB\overline{C}D + ABCD$ [2 marks]

b. Simplify the following logic function using Karnaugh map.
   iii. $f(A,B,C,D) = (1,5,9,10,11,13,14,15)$ [3 marks]
   iv. $f(A,B,C,D) = (0,1,2,5,6,7,8,9)$ [3marks]

c. Implement the simplified logic function obtained in
   v. (Q7.a.i) using two input NAND gates. [5 marks]
   vi. (Q7.a.ii) using two input NOR gates. [5 marks]

Q8. Design a synchronous binary counter that counts the sequence 0 → 1 → 3 → 7 → 5 → 9 → 0.

Design the synchronous counter, considering all other values, other than those given in the sequence cannot occur. Draw the relevant circuit using JK flip-flops and any other required gates.

[20 marks]