THE OPEN UNIVERSITY OF SRI LANKA
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

Final Examination – 2015/2016

ECX4150 – ELECTRONICS - II **(Closed Book)**

DATE: November 17, 2016 ***TIME: 13:30-16:30 hrs.***

ANSWER ANY FIVE (5) QUESTIONS ONLY (each question carries 100 marks)

Be neat and clear. Show all steps very clearly. Underline your final answers wherever possible.

Q1.

Design a synchronous counter (choose an appropriate number of bits for the counter) that counts repeatedly (cycles) through the sequence 0, 3, 5, 7, 6. Use only **JK flip-flops** in your design.

That is, design and come up with the necessary transition table(s) (50 marks), simplified excitation (flip-flop input) equations (i.e., simplified input equations to the flip-flops) (30 marks), and a logic circuit diagram (20 marks) of a synchronous counter circuit that will implement the counting sequence …, (0, 3, 5, 7, 6), (0, 3, 5, 7, 6), (0, 3, 5, 7, 6), …, repeatedly.

Be very neat and clear with your steps, tables, and diagrams.

Q2.

A finite state machine (FSM) is shown in Figure Q2. In the diagram, the input to the FSM is X, and the output is Z. The usual synchronous clock inputs to the flip-flops are assumed, but not shown.

(a) Is this a Moore or Mealy FSM? Explain why? (10 marks)

(b) Showing all necessary steps very clearly, obtain (i) the state-transition table (be very clear and neat) (50 marks), and (ii) the state diagram (be very clear and neat) corresponding to this FSM (25 marks). Note that the flip-flops used in this state machine are all T Flip-flops.

(c) Assuming all flip-flops in this state machine are initially at logic 0, and the input X is the bit sequence 001011001010 (each bit appropriately timed at every clock cycle and sent), determine using your state diagram, the corresponding output bit sequence Z (at each active clock edge) – show (neatly) the output bits of the output sequence aligned with the corresponding input bits of the input bit sequence for clarity. (15 marks)

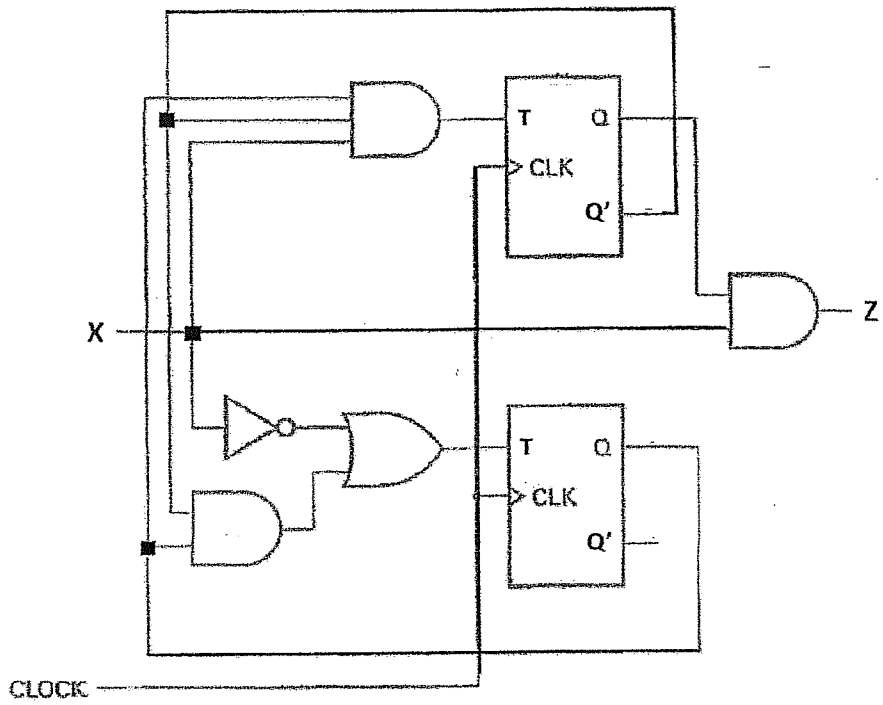

Figure Q2

Q3.

A synchronous sequential circuit (a Finite State Machine – FSM) is to be designed. It has an input "X" and an output "Z". It accepts as input, a (time sequenced) string of bits that are either binary 0 or 1.

The circuit is to produce an output Z = 1 every time a target pattern "1101" occurs in the input bit sequence (which is a long series of bits) applied to its input X. That is, its output is to go to logic 1 when the last four binary digits received are 1101. It is to otherwise output Z = 0.

The target input pattern to be detected **may overlap** itself. This synchronous sequential circuit (sequence detector) is to operate as a Mealy FSM.

Perform the following (be clear and neat, and show all necessary steps):

(i) Draw a neat and clearly labeled state diagram that would correspond to the operation of the above synchronous sequential circuit. (35 marks)

(ii) Derive the state-table and state-transition table (assuming all flip-flops used are to be of **type T**) from the (above) state diagram. You may combine and draw this as a single table. (20 marks)

(iii) Derive the necessary (simplified) excitation equations (flip-flop input) (that is, the necessary combinational-logic input equations to the T flip-flops) (10 marks)

(iv) Derive the necessary (simplified) output-logic equation for this FSM. (10 marks)

(v) Draw the essential features the logic diagram corresponding to this FSM (you do not have to draw the logic gates to the flip-flop inputs but merely state in your diagram the logic equations at the flip-flop inputs). (10 marks)

(vi) How would your state diagram look like, if the input pattern to be detected **may NOT overlap** itself? (15 marks)

Q4.

(a) Show that the maximum efficiency of a Class A power amplifier is 25%. (15 marks)

(b) Show that the maximum efficiency of a Class B power amplifier is 78.5%. (15 marks)

(c) What is the shortcoming of a Class B power amplifier that is overcome by a class AB power amplifier? (10 marks)

For the remaining parts of this problem, use a standard Class B amplifier diagram, if needed. Show all necessary steps and work very clearly.

(d) (i) For a class B power amplifier with a power supply of $V_{cc} = 30V$, providing an 24V peak signal to a 16 ohm load, determine the input power, output power, and circuit efficiency. (8+8+4 marks)

(ii) For the above amplifier ($V_{cc} = 30V$), providing a 6V peak signal (instead of a 24V peak signal) to the same 16 ohm load, determine the input power, output power, and circuit efficiency. (8+8+4 marks)

(ii) Determine the maximum input power, maximum output power, and the maximum efficiency of the above amplifier circuit if $V_{cc} = 30V$ and the load resistance is 16 ohms. (8+8+4 marks)

Q5.

(i) Determine the DC bias conditions (I_B, I_C, and V_{CE}) for the swamped amplifier circuit shown in Figure Q5. Use the exact analysis technique. The dc, ac β values for the transistor are shown in the diagram ($\beta_{dc} = 150$, $\beta_{ac} = 175$). (15 marks)

(ii) Determine the value of the ac emitter-resistance parameter r'_e based on the DC bias operating conditions. (10 marks)

(iii) Use the r-parameter equivalent circuit and perform the following (β_{dc} = 150, β_{ac} = 175):

(a) Determine the dc collector voltage (dc, ac β values are as shown/given) (25 marks)
(b) Determine the ac collector voltage (dc, ac β values are as shown/given) (30 marks)
(c) Draw in a suitable manner, (i) the total collector voltage waveform (10 marks), and (ii) the total output voltage waveform (10 marks)

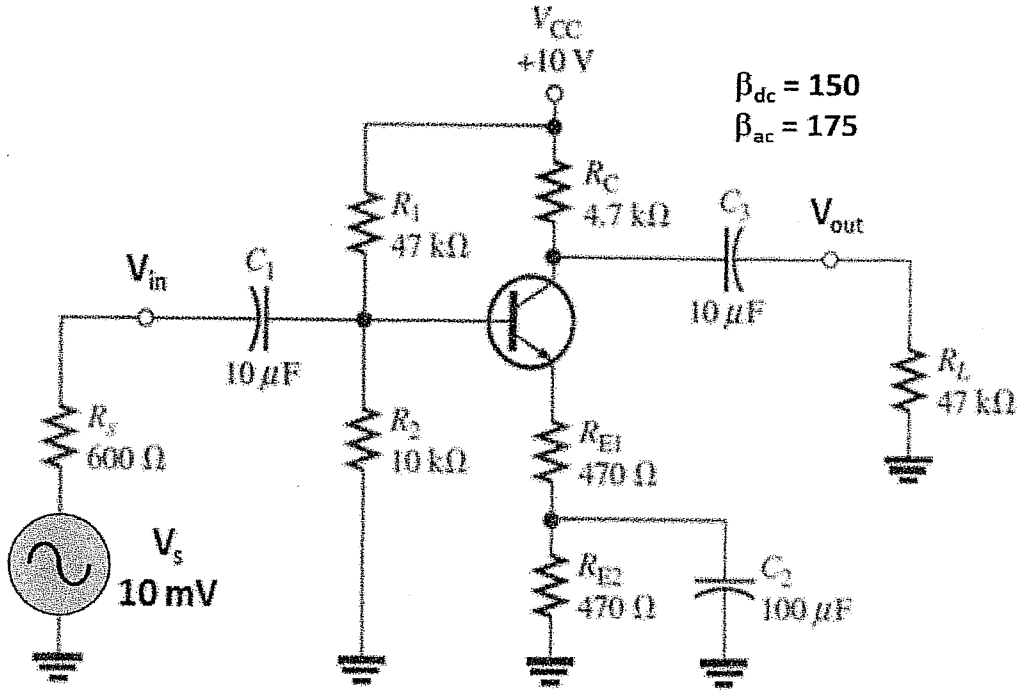

Figure Q5

Q6.

Note: The transfer function of a second-order low-pass filter with dc gain A and cut-off frequency ω_0 rad/sec is given by $H(s) = A\frac{{\omega_0}^2}{s^2+b\omega_0 s+{\omega_0}^2}$ where "b" is a constant.

(a) (i) Show that the transfer function H(s) of a low-pass, Sallen-Key active filter shown in Figure Q6 is given by $H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{s^2R^2C_1C_2+2RC_2s+1}$ (30 marks)

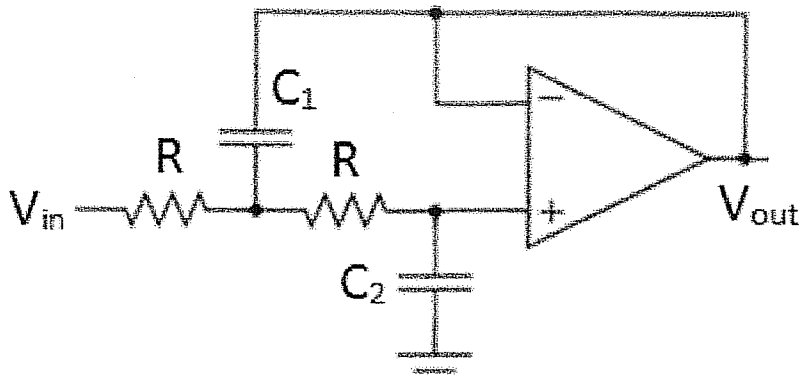

Figure Q6

(ii) What is its dc gain (in terms of some or all of its circuit parameters R, C_1 and C_2)? Show all necessary steps. (15 marks)

(iii) What is its cut-off frequency (rad/sec) in terms of some or all of its circuit parameters R, C_1, and C_2? Show all necessary steps. (15 marks)

(b) The transfer function of a second-order, unity gain, low-pass Butterworth filter with a cut-off frequency of ω_0 rad/sec is given by $H(s) = \frac{{\omega_0}^2}{s^2+b\omega_0 s+{\omega_0}^2}$, where b = 1.414 (square root of two).

Using the above Sallen-Key configuration, design a second-order, unity gain, low-pass (active) Butterworth filter with a cut-off frequency of 3 kHz (40 marks). That is, determine the required circuit configuration (which is the above) and suitable circuit parameters R, C_1, and C_2 to meet problem requirements.

In your design, pick/use a suitable 1% tolerant standard (commercial) value in the practical range of 1KΩ through 1MΩ for the resistor R, and suitable 5% tolerant standard (commercial) values in the practical range 100 pF through 100 nF for the capacitors C_1 and C_2.

Q7.

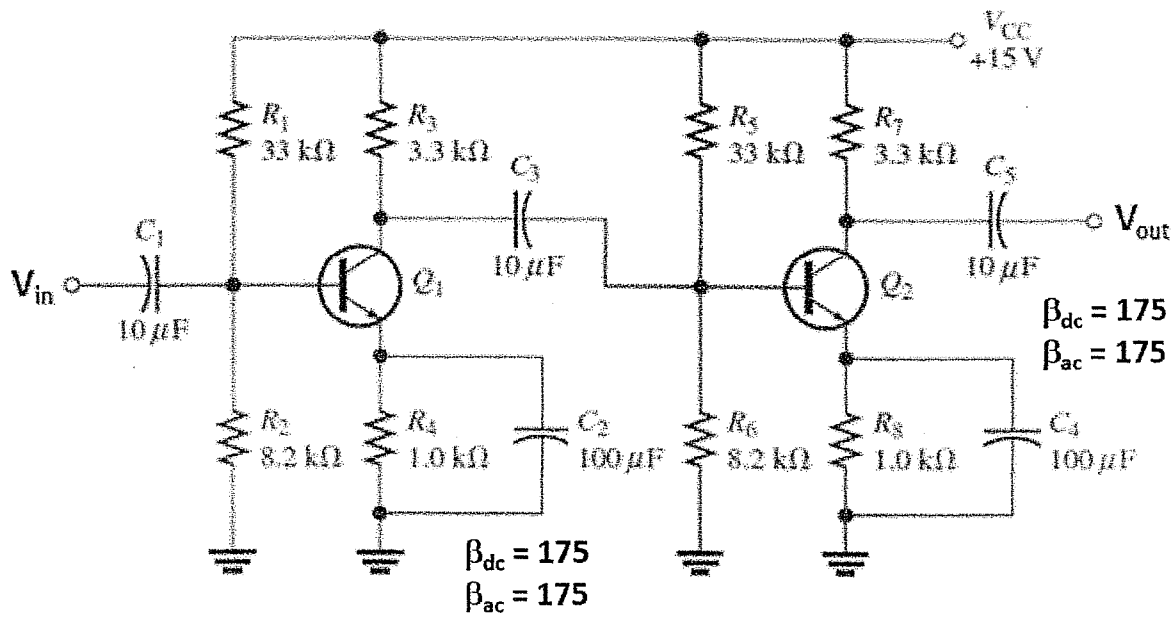

Figure Q7

(a) Determine the dc bias conditions (I_B, I_C, and V_{CE}) for each of the two stages of the two-stage amplifier circuit shown in Figure Q7 ($\beta_{dc} = \beta_{ac} = 175$). Use the exact analysis technique (20 marks).

(b) Determine the value of the ac emitter-resistance parameter r'_e for each stage, based on their DC bias operating conditions. (5+5 marks)

(c) Determine the (mid-frequency) voltage gain of each of the two stages of the above two-stage amplifier circuit (30 + 30 marks), and (b) hence compute its overall voltage-gain (10 marks).

Use the r-parameter model for the transistors.

Assume $\beta_{ac} = \beta_{dc} = 175$. Also, assume that the bypass capacitors and all coupling capacitors have negligible reactances at the frequencies in which the amplifier is operated.

Q8.

For the operational amplifier circuit shown in Figure Q8, compute the output voltage V_Z in terms of the input voltages V_x and V_y (see Figure Q8). Assume that the operational amplifiers used are ideal. Show all steps very clearly. (100 marks)

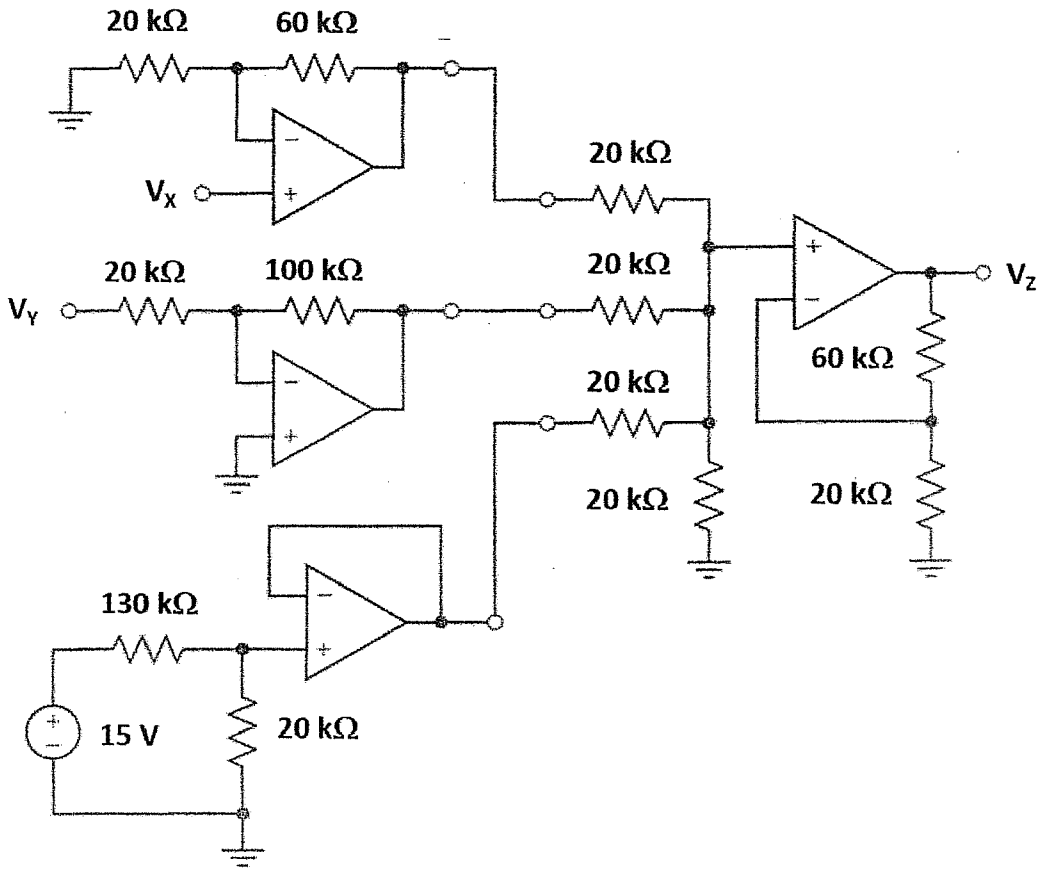
20 kΩ
60 kΩ
V_X
20 kΩ
20 kΩ
100 kΩ
V_Y
20 kΩ
V_Z
60 kΩ
20 kΩ
20 kΩ
20 kΩ
130 kΩ
15 V
20 kΩ

Figure Q8