THE OPEN UNIVERSITY OF SRI LANKA
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
BATCHELOR OF TECHNOLOGY-LEVEL 3

FINAL EXAMINATION - 2015/2016

ECX3150 – Electronics I **(Closed Book)**

Answer any five questions.

Date 16.11.2016 ***Time: 09:30-12:30 hrs.***

Q1. (a) Considering the behavior of the P-N junction in reverse and forward biased modes derive the characteristic curve of a diode. **(4Marks)**

(b) Consider the circuit in Figure Q1 where Z is a Zenner diode with a breakdown voltage of 5.7V and a D near-ideal Si diode with a forward voltage drop of 0.7V.

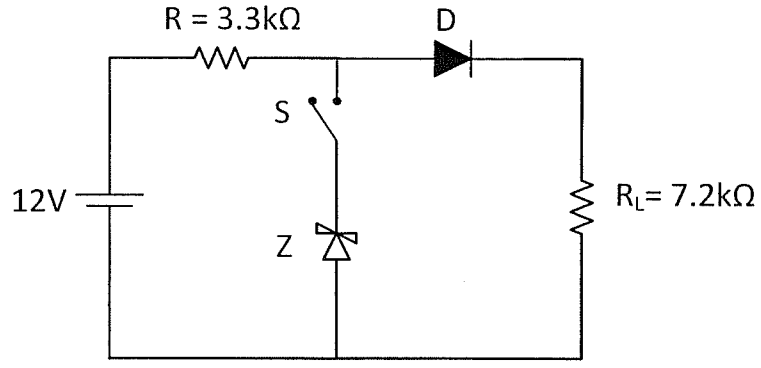

Figure Q1

i. Let switch (S) be open initially. Calculate the voltage across the load resistance R_L. **(4marks)**

ii. Calculate the voltage across load resistance R_L when S is closed. **(4marks)**

iii. Calculate the current through R_L when S is closed. **(2marks)**

iv. Hence calculate the current flowing through the Zenner diode. **(6marks)**

Q2. Consider the DC power supply circuit in Figure Q2.

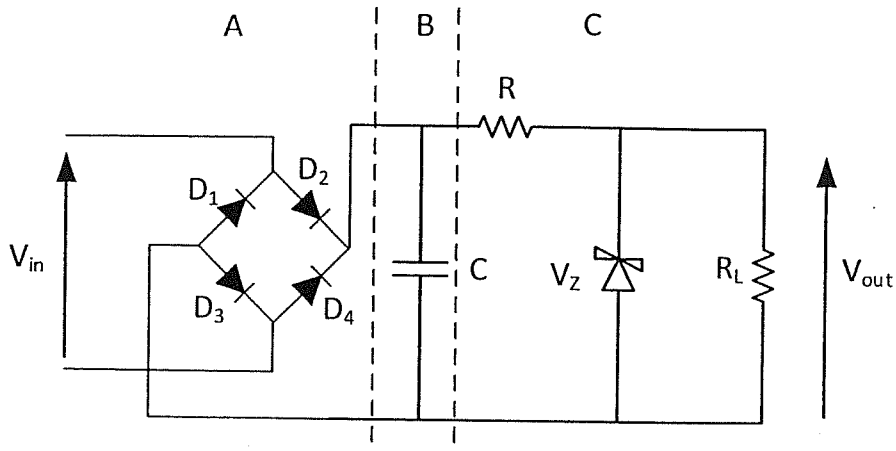

Figure Q2

Let $D_1 \sim D_4$ are identical Si diodes with a forward voltage drop of $0.7V$ in each. $R = 1k\Omega$, $R_L = 10k\Omega$, $C = 10\mu F$. Zenner diode breakdown voltage $V_Z = 5.1V$. V_{in} is a sinusoidal voltage with a peak amplitude of 9V.

(a) Identify the three distinct sub-circuits A, B and C. **(3Marks)**

(b) Assuming that minimum output value of the section B is 6.1V, draw the output waveforms at the outputs of each A, B and C. **(6Marks)**

(c) Calculate the minimum and maximum currents flowing through the Zenner diode. **(8Marks)**

(d) Hence calculate the minimum power rating of the Zenner diode. **(3Marks)**

Q3. The single stage BJT transistor amplifier circuit shown in Figure Q3 consists of a Si transistor ($V_{be} = 0.7V$) with a current gain, $\beta = 100$.

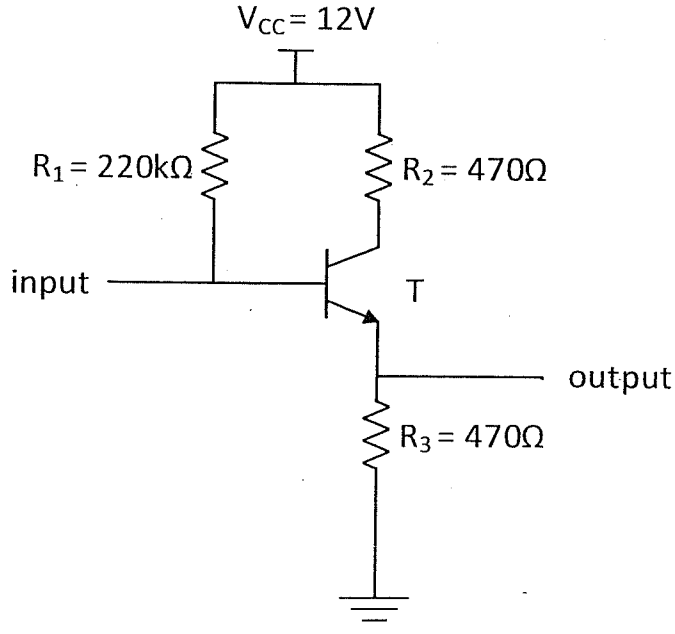

Figure Q3

(a) Write the bias configuration of the circuit shown in Figure Q3. **(2Marks)**
(b) Calculate the base, collector and emitter currents of the transistor. **(6Marks)**
(c) Hence calculate the V_{CE} voltage. **(4Marks)**
(d) Draw the DC load line for the circuit. **(6Marks)**
(e) Hence, comment on the stability of the amplifier in Figure Q3. **(2Marks)**

Q4. Figure Q4 shows a FET based cooling fan motor (M) driver circuit. T is a thermistor which decreases its resistance when the temperature is increased and vise-versa.

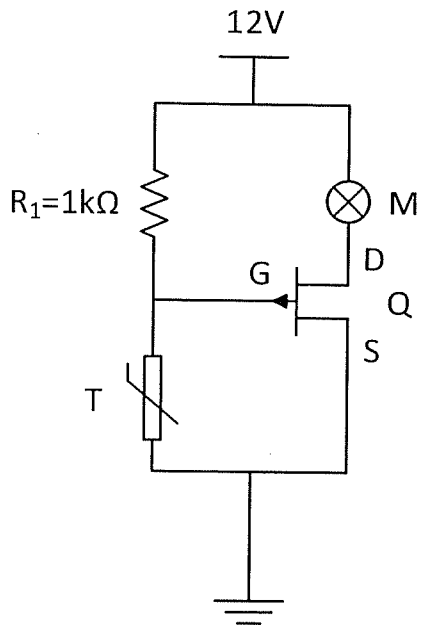

Figure Q4

(a) Using a clear diagram, explain the phenomena of *pinch-off* in a JFET. **(5Marks)**
(b) What is the bias configuration used in this circuit in Figure Q4? **(2Marks)**
(c) If the pinch-off voltage of the FET (Q) in Figure Q4 is $3V$ and $I_{DSS} = 12mA$, calculate the drain - source current through the FET for thermistor resistances of
  i. 100Ω
  ii. 333.33Ω
  iii. $1k\Omega$. **(3x3marks)**

(d) Hence explain the behavior of the FET (Q) when the temperature changes from 30 to 60 degrees (as a result resistance changes from $1k\Omega$ to 100Ω) **(4Marks)**

Q5.

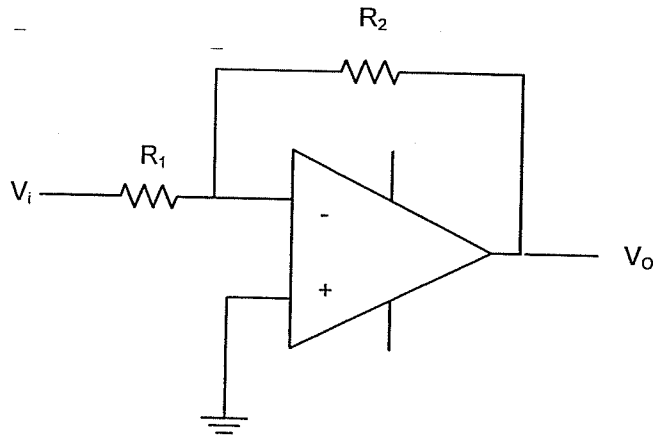

Figure Q5 (a)

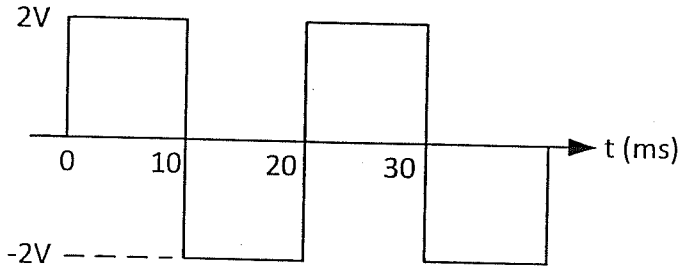

Figure Q5 (b)

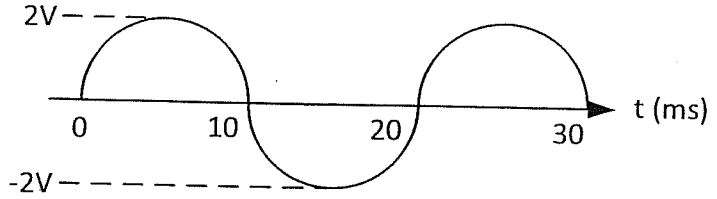

Figure Q5 (c)

(a) List four properties of an ideal operational amplifier. **(4Marks)**

(b) Derive an expression for the $\frac{V_o}{V_i}$ in the ideal operational amplifier based circuit in Figure Q5 (a). **(6Marks)**

(c) Let $R_1 = 2.2k\Omega$ and $R_2 = 4.7k\Omega$. Draw the output waveforms with respect to the input signals given in Figures Q5 (b) and Q5 (c). **(2x5Marks)**

Q6.

(a) Perform the following conversions.

i. 9.75_{10} to binary
ii. 0.2_{10} to binary
iii. $CC.F_{16}$ to octal
iv. -23 to 8 bit 2's complement **(4x2Marks)**

(b) Find the addition of the two BCD numbers 10010011.0101 and 00110111.0001. **(4Marks)**

(c) Perform the calculation 12-15 in 8 bit 2's complement arithmetic. **(4Marks)**

(d) Using binary division, divide 100011_2 by 110_2. **(4Marks)**

Q7.

(a) Using a truth table, prove the Boolean identity $ABC + AB\bar{C} + A\bar{B}\bar{C} + A\bar{B}C = A$ **(4Marks)**

(b) Using De Morgan's theorem prove following identities.

i. $AB + \bar{B}C = \overline{(\bar{A} + \bar{B})(B + \bar{C})}$ **(3Marks)**
ii. $(\bar{A} + \bar{C})(B + \bar{C})[A + B(\bar{B} + \bar{C})] = AC + \bar{B}C + \bar{A}(\bar{B} + BC)$. **(4Marks)**

(c) Implement the Boolean function $F = (A + \bar{B})(\bar{C} + D)$ using

i. NOT, AND and OR gates
ii. NAND gates only
iii. NOR gates only. **(3x3Marks)**

Q8.

(a) A three variable Boolean logic expression is given by $E = \prod M(2,4,6)$. Using Karnaugh maps find,

i. minimum POS and
ii. minimum SOP expressions. **(10Marks)**

(b) Construct Karnaugh maps for the expression $F = ABC + \bar{A}BC + AB\bar{C}$ and find

i. minimum SOP and
ii. minimum POS expressions. **(10Marks)**