## THE OPEN UNIVERSITY OF SRI LANKA

Faculty of Engineering Technology
Department of Electrical & Computer Engineering



**Bachelor of Technology Honors in Engineering** 

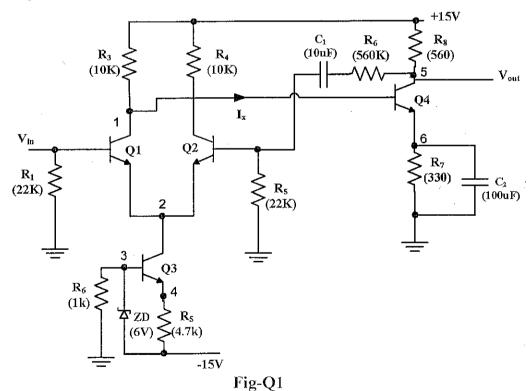
## Final Examination (2016/2017) ECX4230: Fault diagnosis in Electronic circuits

Date: 10<sup>th</sup> November 2017 (Friday)

Time: 9:30 am - 12:30 am

Answer any five questions. All symbols and notation have their usual meaning.

Q1. Consider the amplifier shown in Fig-Q1. The Q1, Q2 and Q3 are of high gain transistors. The current gain of Q4 is 50.



a) Calculate the Ix and the test point voltages at no Signal. Do not assume any voltage for a test point. [8 marks]

b) A sine wave signal of 1kHz with 145 mV amplitude is applied to the input. Sketch the output signal with the input to a common time scale. Mark the time and voltage values where necessary.

[4 marks]

c) Following table shows the test point voltages (T.P) under faulty conditions. Identify the faulty component/s with fault type by giving reasons. [8 marks]

Case	T.P 1	T.P 2	T.P 3	T.P 4	T.P 5	T.P 6	Output
A	5.4	-0.6	-9	-9.6	15	4.8	No output
В	5.4	-0.6	0	-0.6	15	4.8	No output
С	4.8	-0.6	-9	-9.6	15	4.2	No output
D	3.2	-0.6	-9	-9.6	7	2.6	No output

Q2.

- a) State the advantages and the disadvantages of linear regulators over switch mode regulators. [5 marks]
- b) A DC power supply is shown in Fig-Q2.

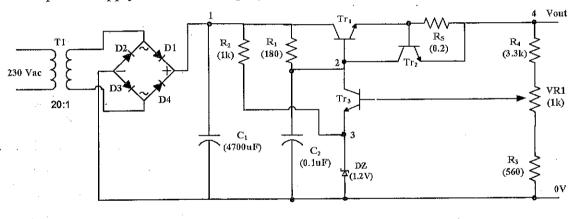


Fig-Q2

i. Calculate the range of the output voltage.

- [4 marks]
- ii. Is it possible to use this supply for a 27W load at 9V? Justify your answer.

  If your answer is 'No', Show how you are going to modify the circuit to achieve the requirement.

  [3 marks]
- iii. Following table shows the voltages at the test points under fault conditions. Find the faulty component/s and the fault type by giving reasons. Assume VR1 is set to give the output 9V. [8 marks]

Case	T.P 1	T.P 2	T.P 3	T.P 4
A	11.5	3	1.2	1.8
В	11.5	0	1.2	U
C	11.5	10	0	0
D	8	6.2	1.2	5

Q3.

a) Safe the use of Schmitt trigger in electronic circuits.

[2 marks]

b) The circuit shown in Fig-Q3 uses a Schmitt trigger with a JFET.

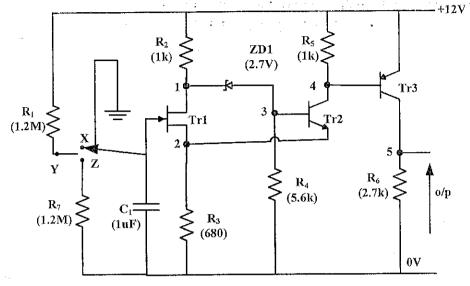


Fig-Q3

- i. Assume the JFET starts to conduct when  $V_{GS} > -1$  and when the JFET is 'ON', its  $V_{DS}$  is 1V. Calculate the threshold voltages of  $V_G$  at which the output of the circuit will change. [4 marks]
- ii. Calculate the test point voltages for the two states of the output. Assume  $V_{\text{CE}}$  sat for Tr2 and Tr3 is 0.2V. [4 marks]
- iii. The switch is initially at position X. If it is turned to position Y for one second and then turned to position Z, Calculate the width of output signal. [4 marks]
- iv. Following table shows three fault cases with the measured test point voltages when the switch is at position A. State faulty component/s with fault type by giving reasons.

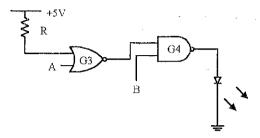
  [6 marks]

Case	T.P 1	T.P 2	T.P 3	T.P 4	T.P 5
Α	10.1	6.8	7.4	2.0	0
В	6.3	3.5	4.1	11.4	11.8
С	6.5	3.2	3.8	12.0	0

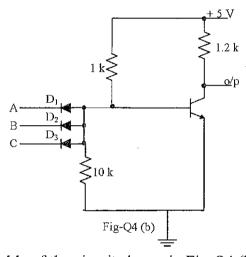
Q4.

a) Explain the use of logic probe and logic pulsar to test the circuit shown in Fig-Q4(a).

[4 marks]



b) Consider the logic circuit shown in Fig-Q4 (b).



i. Give the truth table of the circuit shown in Fig-Q4 (b).

[8 marks]

ii. State the logic function of the circuit.

[2 marks]

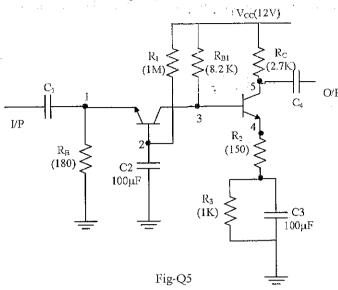
iii. Indicate the corresponding observations of the logic probe on the output Q for the following faults for the input conditions. [6 marks]

Fault 1: D<sub>1</sub> open circuited

Fault 2: 1 k resistor open circuited

Fault 3: D<sub>3</sub> short circuited

Q5. A two-stage amplifier is shown in Fig -Q5.



- a) If the value of  $\beta$  for both transistors is 100, calculate the test point voltages at no signal. Do not assume for maximum output swing. [7 marks]
- b) When 1 mV peak to peak sine wave input is fed to the amplifier, the signal observed at test point 3 is 0.238V peak to peak. Calculate the amplitude of the signal voltage observed at the output. [5 marks]
- c) Following voltages readings of the test points are observed from a DVM under faulty conditions. Identify the faulty component/s with fault type giving reasons.

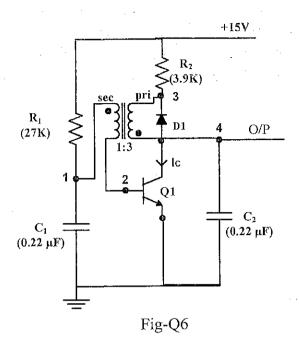
  The readings are in volts unless otherwise stated. [8 marks]

Case	T.P 1	T.P 2	T.P 3	T.P 4	T.P 5	Output
A	2.1 mV	0.6	4.1	3.5	3.7	No output
В	0.2	0.8	1.0	0.4	0.6	No output
С	0.2	0.8	1.2	0.6	0.8	No output
D	0.2	0.8	2.8	0	12	No output

Q6.

a) An amplifier of open loop A0 is supplied with positive feedback. If the feedback ratio is  $\beta$ , find an expression for the overall gain. What will happen when  $\beta A_0 = 1?$  [5 marks]

b) The circuit shown in Fig-Q6 is a blocking oscillator.



- i. When transistor is switched on, sketch the waveforms  $V_{34}$ ,  $V_2$  and  $V_4$  on a common time scale for two cycles. [6 marks]
- ii. Estimate the approximate lowest frequency of the output signal. [3 marks]
- iii. Sate the faulty component/s and fault type with reasons for the following.
  - A. If the oscillator produces negative going pulses of short period.
  - B. If the frequency of oscillation is correct but the amplitude of the output pulse is small.
  - C. If the observed voltages of the test points are,

Case	<b>T.P 1</b>	T.P 2	T.P 3	T.P 4	output
A	0.7	0.7	0.4	0.2	No output
В	0.7	0.7	15	15	No output

[6 marks]

Q7.

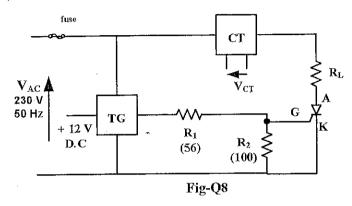
- a) Explain how the detected Y and colour component signals are used to recover the colour signals R G and B in a PAL receiver. [5 marks]
- b) How does the receiver colour decode carrier signal is kept in phase with the transmitter colour encoder carrier signal. [5 marks]
- c) What are the main sections of a tuner in a TV receiver? Explain the function of each section. [5 marks]
- d) In a defective TV receiver sound signal is receiving. Explain what sections are likely to be faulty and method that you are going to follow to identify the faulty section.[5 marks]

Q8. A thyristor power control circuit is shown in Fig-Q8. The trigger circuit (TG) produces a pulse train  $V_x$  synchronized to  $V_{AC}$ . The current in load is sensed by the device CT and  $V_{CT}$  is proportional to the load current. Forward voltage drop of the thyristor and gate power dissipation are 2V and 300mW respectively. The specifications of the trigger circuit are,

Pulse height – 12 V

Maximum pulse current – 70 mA

Pulse width – 100 μs



- a) If the load RL can vary between 100  $\Omega$  to 10 K $\Omega$ , Find following specifications for the thyristor
  - i. Maximum valves of

Forward rms current

Gate pulse current

Gate pulse voltage

ii. Minimum value of

Peak reverse voltage

Forward rms current

[6 marks]

b) Under a faulty condition, following observations are made. Determine the most obvious fault and state reasons for your answer. [5 marks]

VAK - 230 V

VX(pulse height) – 12V

Vg (pulse height) - 3V

c) Design a circuit which can be used to produce a pulse train to trigger the thyristor. Sketch the voltages at  $V_{AC}$ ,  $V_{CT}$ . [8 marks]