00170

THE OPEN UNIVERSITY OF SRI LANKA
Faculty of Engineering Technology
Department of Electrical & Computer Engineering

Bachelor of Technology Honours in Engineering

Final Examination (2016/2017)
ECX4150: Electronics II

Date: 9th November 2017 (Thursday) **Time: 1:30 pm – 4:30 pm**

Answer any **five (5)** questions only, out of eight questions. All questions carry equal marks.

Underline your answers. Be neat, show all work.

Q1. Answer the following:

(a) Show that the maximum efficiency of a Class A power amplifier is 25%. (16 marks)

(b) Show that the maximum efficiency of a Class B power amplifier is 78.5%. (16 marks)

(c) What is the shortcoming of a Class B power amplifier that is overcome by a class AB power amplifier? (8 marks)

For the remaining parts of this question, consider a standard Class B amplifier diagram if needed. Show all necessary steps and work very clearly.

(d) (i) For a class B power amplifier with a power supply of V_{cc} = 24 V, and providing an 18V peak signal to a 16 ohm load, determine the input power, output power, and circuit efficiency. (8 + 8 + 4 marks)

(ii) For the above amplifier (V_{cc} = 24 V), providing a 10 V peak signal (instead of an 18V peak signal) to the same 16 ohm load, determine the input power, output power, and circuit efficiency. (8 + 8 + 4 marks)

(ii) Determine the maximum input power, maximum output power, and the maximum efficiency of the above amplifier circuit (V_{cc} = 24 V, and the load resistance is 16 ohms). (8 + 8 + 4 marks)

Q2.

A two-stage amplifier shown in Figure Q2. Assume that the transistors are of silicon, and that $\beta_{dc} = \beta_{ac} = 150$ for each transistor (Q1 and Q2) used in the amplifier circuit. Answer the following:

(a) Determine the dc bias conditions (I_B, I_C, and V_{CE}) for each of the two stages of the two-stage amplifier circuit shown in Figure Q2. Use the exact analysis technique. (15 marks).

(b) Use the r-parameter model to answer the following:

(i) Determine the value of the ac emitter-resistance parameter r'e for each stage, based on their DC bias operating conditions. (10 marks)

(ii) Determine the (mid-frequency) voltage gain of each of the two stages of the above two-stage amplifier circuit. (30 + 30 marks) \

(iii) Determine the overall voltage gain of the two-stage amplifier. (10 marks)

(iv) Express the voltage gains found in parts (c) and (d) (above) in dB. (5 marks)

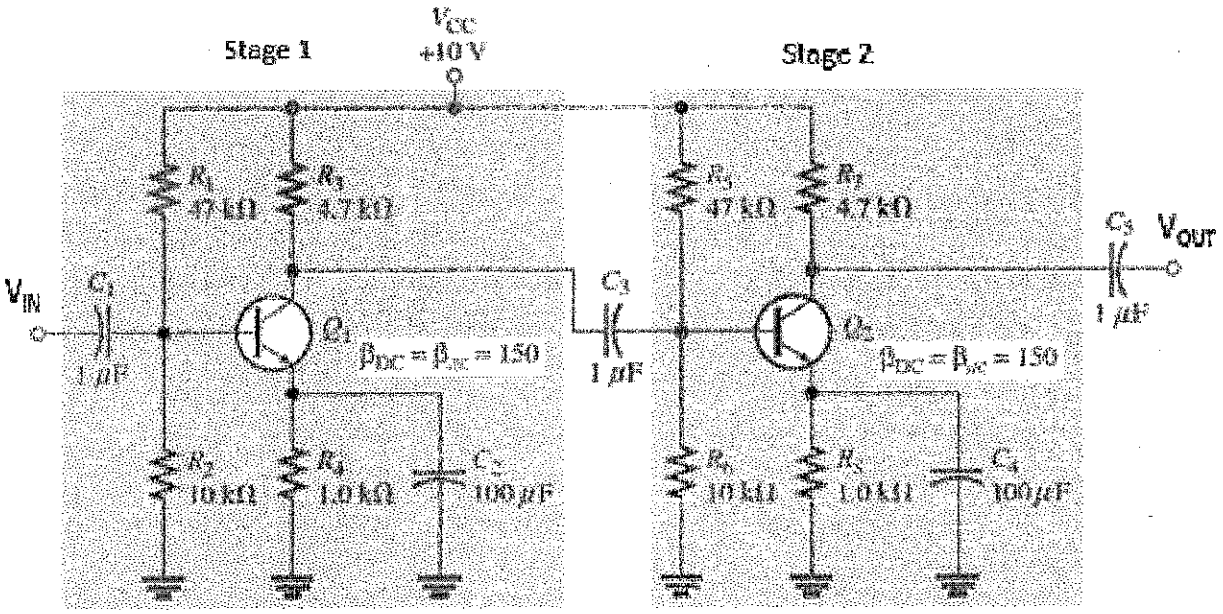

Figure Q2

Q3.

(a) Explain briefly using figure(s) as necessary, what is meant by the term hysteresis. Provide an example situation where it is beneficially used (5 + 5 marks).

(b) (i) For the Schmitt trigger circuit shown in Figure Q3, the positive and negative supply voltages are +15V and -15V respectively, and $V_{Ref} = +6V$. Find (1) the upper and lower trigger levels for the circuit, and (2) the amount of its hysteresis. (20 + 20, + 10 marks)

(ii) Sketch neatly and clearly the V_{out} versus V_{in} transfer characteristics for the above, marking all key values and providing all necessary labels. (20 marks)

(iii) Draw the output waveform that would result when the input is a 10V peak sine-wave. (20 marks)

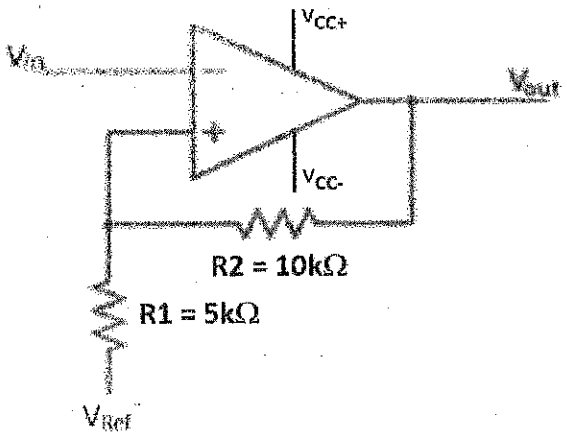

Figure Q3

Q4.

A swamped amplifier circuit is shown in Figure Q4.

The transistors are of silicon and their gains are $\beta_{dc} = 150$, and $\beta_{ac} = 175$.

(a) Using an exact analysis technique, determine the DC bias conditions (I_B, I_C, and V_{CE}) for the circuit shown in Figure Q4. (15 marks)

(b) Determine the value of the ac emitter-resistance parameter r'_e based on the DC bias operating conditions. (10 marks)

(c) Using the r-parameter equivalent circuit for the swamped amplifier circuit shown in Figure Q4 (same figure as above), perform the following for the same:

(i) Determine the dc collector voltage. (15 marks)
(ii) Determine the ac collector voltage. (20 marks)
(iii) Draw the total collector voltage waveform and the total output voltage waveform. (20 + 20 marks)

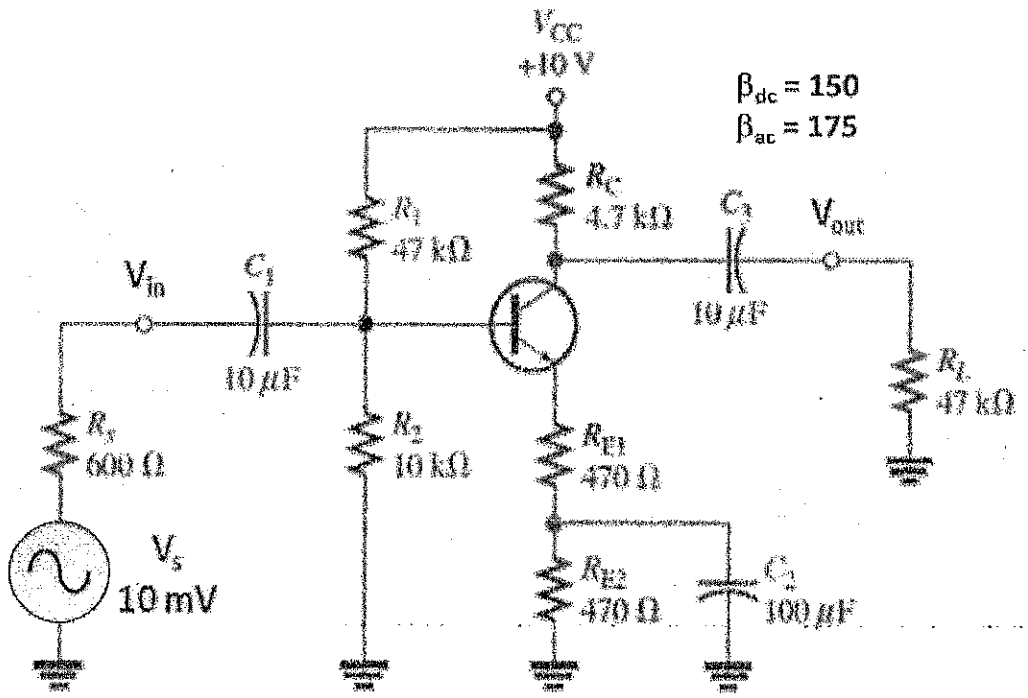

Figure Q4

Q5. (50 marks)

(a) Using the "Low-Pass Butterworth Denominator Polynomial" table (ω_0 = 1 rad/sec) given below, determine the transfer function of a **fourth order**, low-pass Butterworth filter with a unity gain and a cut-off frequency of ω_0 rad/sec. Write in "standard" form. (20 marks)

n (order)	Normalized Denominator Polynomials in Factored Form
1	$(1+s)$
2	$(1+1.414s+s^2)$
3	$(1+s)(1+s+s^2)$
4	$(1+0.765s+s^2)(1+1.848s+s^2)$
5	$(1+s)(1+0.618s+s^2)(1+1.618s+s^2)$
6	$(1+0.518s+s^2)(1+1.414s+s^2)(1+1.932s+s^2)$
7	$(1+s)(1+0.445s+s^2)(1+1.247s+s^2)(1+1.802s+s^2)$
8	$(1+0.390s+s^2)(1+1.111s+s^2)(1+1.663s+s^2)(1+1.962s+s^2)$
9	$(1+s)(1+0.347s+s^2)(1+s+s^2)(1+1.532s+s^2)(1+1.879s+s^2)$
10	$(1+0.313s+s^2)(1+0.908s+s^2)(1+1.414s+s^2)(1+1.782s+s^2)(1+1.975s+s^2)$

Table: Low-Pass Butterworth Denominator Polynomial with Cutoff Frequency of 1 rad/sec and Different Filter Orders

(b) Draw a neat circuit diagram of a second order low-pass Sallen-Key operational-amplifier based filter circuit having equal resistance values and different capacitor values. (10 marks)

(c) The transfer function H(s) of a low-pass, Sallen-Key active filter circuit having equal resistance values and different capacitor values is given by $H(s) = \frac{1}{s^2R^2C_1C_2+2RC_2s+1}$

Design a **fourth-order**, unity gain, low-pass (active) Butterworth filter with a cut-off frequency of 3500 Hz by cascading second-order low-pass Sallen-Key operational-amplifier based filter sections. That is, determine (draw neatly) the required circuit configuration (which is the above cascaded circuit configuration), and suitable values for all circuit parameters to meet the requirements of the problem. Show all work. (20 + 50 marks)

For your design, pick/use a suitable 1% tolerant standard values in the range 1KΩ through 1MΩ for the resistors, and a suitable 5% tolerant standard values in the range 100 pF through 100 nF for the capacitors.

Q6.

A finite state machine (FSM) is shown in Figure Q6. In the diagram, the input to the FSM is X, and the output is Z. The usual synchronous clock inputs to the flip-flops are assumed, but not shown.

(a) Is this a Moore or Mealy FSM? Explain why? (10 marks)

(b) Showing all necessary steps clearly, obtain (i) the state-transition table (be clear and neat), and (ii) the state diagram (be clear and neat) corresponding to this FSM. Note that the flip-flops used in this state machine are all T Flip-flops. (50 + 25 marks)

(c) Assuming all flip-flops in this state machine are initially at logic 0, and the input X is the bit sequence 001011001010 (each bit appropriately timed at every clock cycle and sent), determine using your state diagram, the corresponding output bit sequence Z (at each active clock edge) – i.e., show (neatly) the output bits of the output sequence aligned with the corresponding input bits of the input bit sequence for clarity. Be neat for full credit (15 marks)

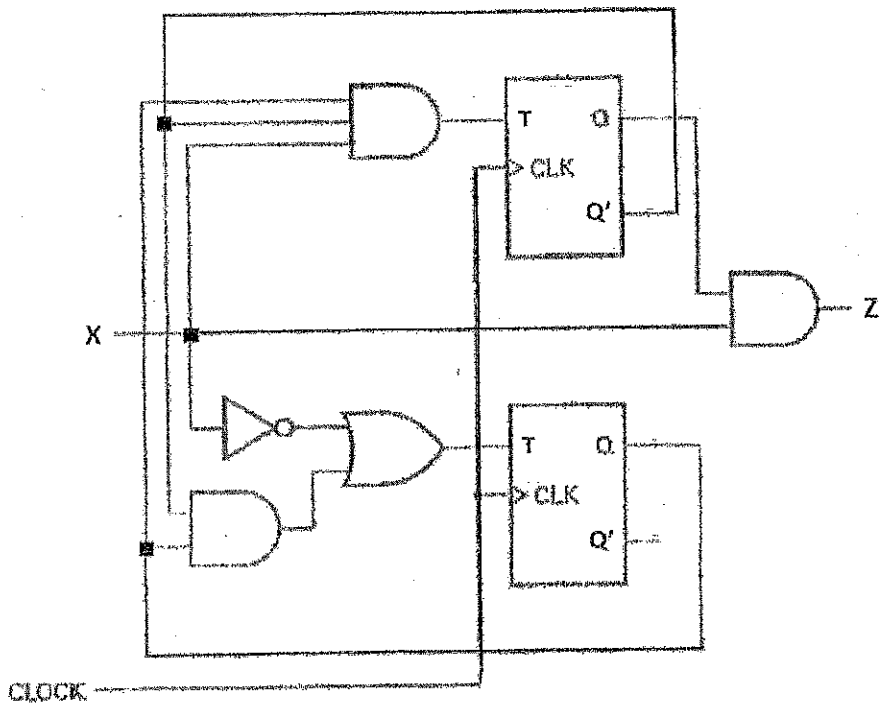

Figure Q6

Q7.

A synchronous Finite State Machine (FSM) to be designed has an input "*X*" and an output "Z". It is to produce an output Z = 1 every time the pattern "1001" occurs in the input sequence (which is a long series of bits) applied to its input X. It is to otherwise output Z = 0.

This synchronous sequential circuit (sequence recognizer) to be designed is to operate as a Mealy FSM. You are to use only D flip-flops in the design.

The input pattern that is to be detected **may overlap** itself.

Perform the following (please be neat):

(i) Draw the state diagram that would correspond to the above synchronous sequential circuit. (35 marks)

(ii) Derive the state table and the state-transition table from the (above) state diagram (you may combine the two into one table). (25 marks)

(iii) Derive the needed simplified Boolean expressions to implement the above state table (i.e., in order to draw the logic diagram). (15 marks)

(iv) Draw the logic diagram of a circuit that implements the required synchronous sequential circuit based on the above Boolean expressions. Note: It is sufficient if only the essential features of the logic circuit are shown. You do not have to draw the logic gates to the flip-flop inputs but merely state in your diagram the necessary logic equations at the flip-flop inputs. (10 marks)

(v) How would the state diagram for the synchronous sequential circuit be, if the input pattern that is to be detected **may NOT overlap** itself? (15 marks)

Q8.

Design a synchronous counter (choose an appropriate number of bits for the counter) that counts repeatedly (cycles) through the sequence 0, 4, 7, 2, 3. Use only **JK flip-flops** in your design. (100 marks)

That is, develop the necessary transition table(s) (50 marks), simplified input equations to the flip-flops (30 marks), and a logic circuit diagram (20 marks) of a synchronous counter circuit that will implement the counting sequence …, (0, 4, 7, 2, 3), (0, 4, 7, 2, 3), (0, 4, 7, 2, 3), …, repeatedly.

Be very neat and clear with your steps, tables, and diagrams.