THE OPEN UNIVERSITY OF SRI LANKA
B.Sc DEGREE PROGRAMME: LEVEL 04
FINAL EXAMINATION: 2009/2010
CSU2178: DIGITAL COMPUTER FUNDAMENTALS

DURATION: **TWO AND HALF HOURS** (2 ½ HOURS)

101

Date: 09th July, 2010 Time: 1.30 pm – 4.00 pm

Answer FOUR Questions ONLY.

Q1.

a) Briefly describe the following:

i. Radix number system
ii. Two's complement addition

b) Draw the truth table of a full adder circuit.

c) Implement the full adder circuit using basic logic gates.

d) Convert the following decimal numbers into binary (base 2) and hexadecimal (base 16) numbers.

i. 45 ii. 67

e) By using 12-bit registers, store the above values in part (d).

f) Use two's complement addition to perform the following calculations.

i. 45 + 67 ii. 67 + (- 45) iii. 45 + (- 67) iv. - 67 - 45

Q2.

a) Implement the following gates using 2 input NAND gates only.

i. OR
ii. AND
iii. XOR

b) Consider the following function:

$F = \overline{A}.\overline{B}.\overline{C}.\overline{D} + \overline{A}.\overline{B}.C.\overline{D} + A.\overline{B}C.D + B.C.D + A.B.\overline{C}.D$ and

$A.\overline{B}.\overline{C}.\overline{D} = A\overline{B}.C.D = A.\overline{B}.C.\overline{D} = \overline{A}.B.\overline{C}.D = X$ (Don't care)

i. Draw the truth table for the above function.
ii. Find the minimal expression for the above function, by using the K-MAP method.
iii. Draw a circuit diagram for the above function,

a) by using basic gates. (NOT, 2 input AND, 2 input OR)
b) by using 2 input NAND gates only.

Q3.

a) What is a multiplexer? Describe briefly.

b) Implement 8-to-1 multiplexer by using only two 4-to-1 multiplexers and the basic logic gates.

c) Implement 8-to-1 multiplexer by using a 16-to-1 multiplexer.

d) Consider the following truth table.

A	B	C	D	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

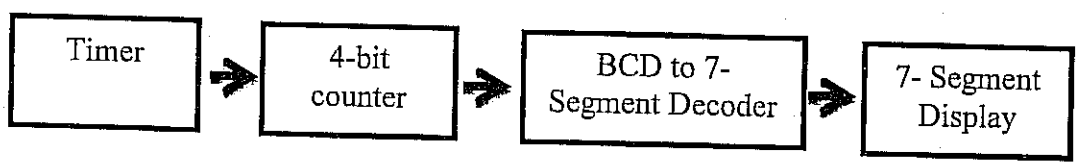
i. Write an algebraic expression for F.
ii. Implement the above truth table by using 16-to-1 multiplexers only.

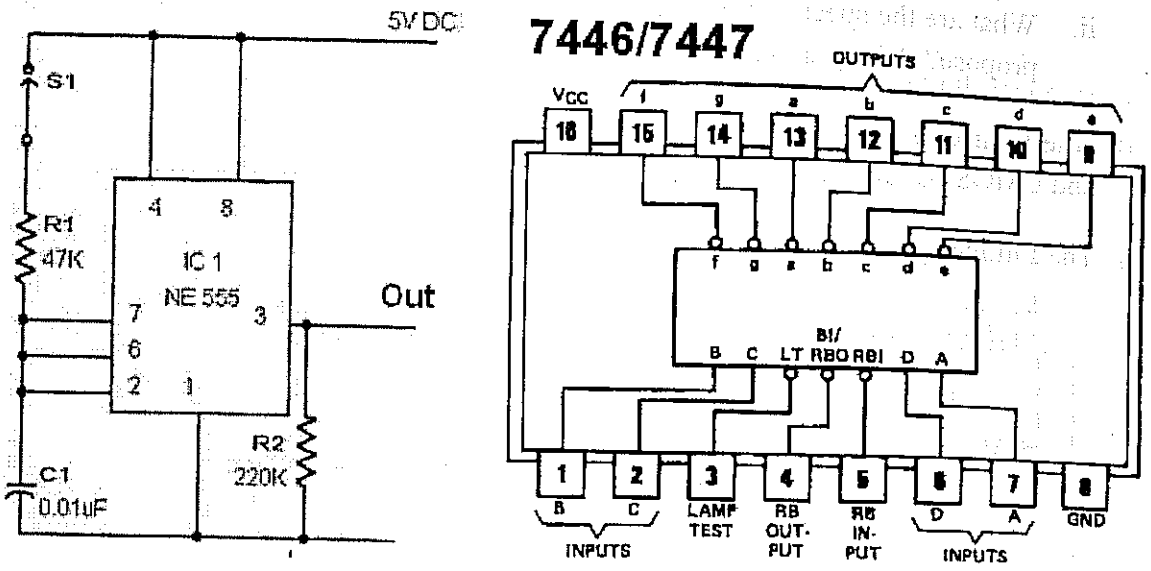
Q4.

a) Briefly describe the following:

i. 7- segment display
ii. J-K flip-flop
iii. BCD to 7- segment decoder

b) You need to design a timer circuit which shows time (0 – 9). Functional diagram of the complete circuit, circuit diagram of the timer and the layout of the BCD to 7-segment decoder are given below.





i. Draw the complete circuit diagram (draw a 4-bit counter by using J-K flop-flops and connect all other components such as timer, BCD to 7- segment decoder and the 7-segment display).

ii. Draw the frequency waveforms for the 4-bit counter designed above.

Q5.

a) Write short notes on the following:

i. Direct mapped cache and associative mapped cache
ii. The memory hierarchy
iii. Disk file system
iv. Level of a machine

b) Using a D type flip-flop, implement the following:

i. Single memory element (with Select, Read and Data in/out)
ii. 4 bit register (with WR, CLK and EN)

Q6.

a) Suppose you need to buy a Personal Computer (PC) for the graphics design propose.

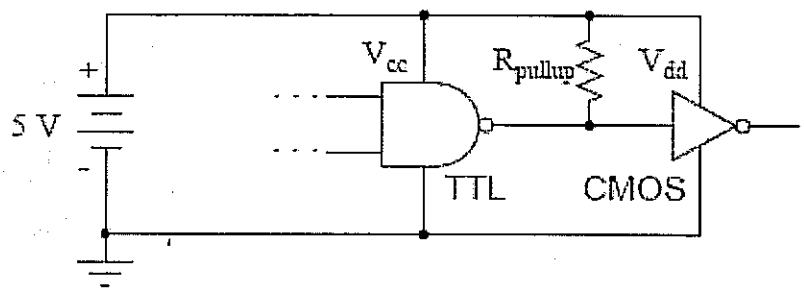
i. Create a specification sheet with the following information.

Specification for the PC	
Processor	Type, clock speed, bus speed , other relevant information
Memory	Type, capacity, bus speed, etc.
Hard Drive	Type, capacity, speed, etc.
Optical device	Type, speed, other options
Graphics	Capacity, type

ii. What are the special options/features you have to consider for graphics designing propose? Briefly describe.

b) Briefly discuss the differences between working speed and the output power of TTL and CMOS IC families.

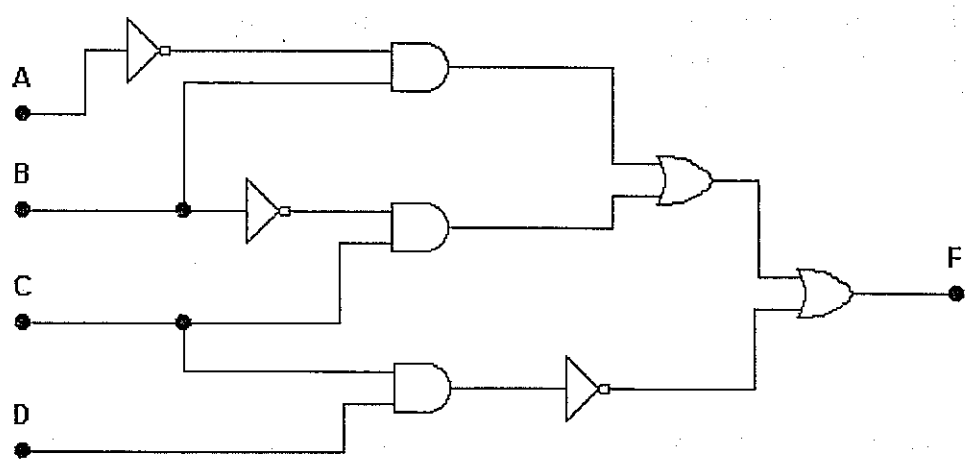
c) The following figure shows the connection between TTL gate and the CMOS gate.



Considering the input and output voltage levels, briefly describe the process of the R_{pullup} resister.

d) Draw an IC circuit for the following digital circuit. (A, B and C are inputs & F is the output)

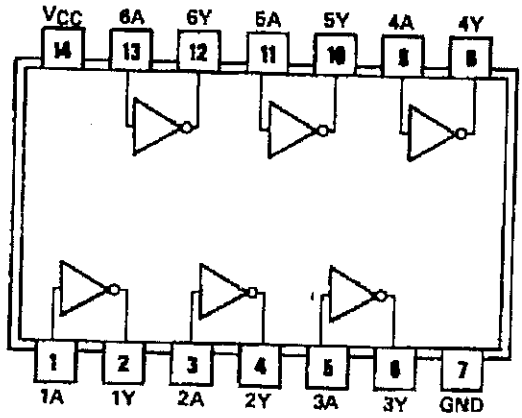
(Hint: use the given Data Sheet.)



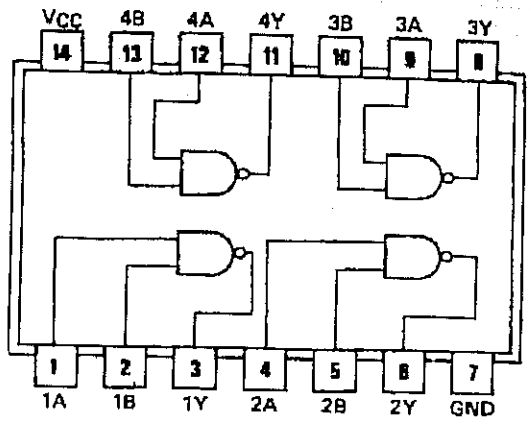
Data Sheets

7404 Hex inverters, 7400 Quad 2-input NAND gates, 7432 Quad 2-input OR gates and 7408 Quad 2-input AND gates.

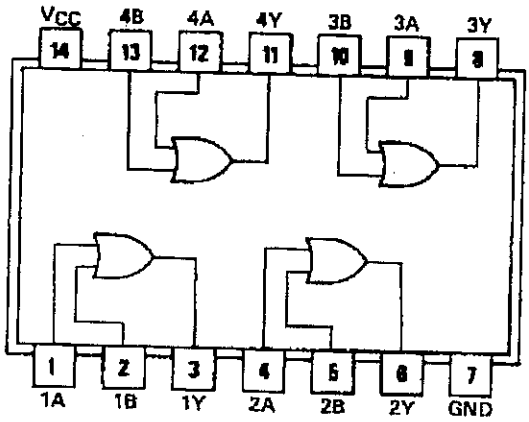
7404



7400



7432



7408