



Date: 25th February, 2010

Time: 4.00 pm – 5.30 pm

Answer ALL questions.

Q1.

- a. "Any logical gate can be implemented by using NAND gate(s)." Explain this statement by using suitable truth tables and logic circuits.
- b. Consider the following truth table and answer the questions from b (i) to b (iv).

A	B	C	D	out
0	0	0	0	X
0	0	0	1	X
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	X
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

- i. Write a logical expression for the above truth table.
- ii. By using the K-MAP method, define the minimal expression for the above expression.
- iii. Draw the logical circuit diagram for the minimal expression in part (ii) above using basic logic gates (NOT, 2 input AND, 2 input OR).
- iv. Draw the logical circuit diagram for the minimal expression in part (ii) above using 2 input NAND gates.

Q2.

- a. Briefly describe the following terms (components) by using functions, truth tables and circuit diagrams.
 - i. Multiplexers
 - ii. J-K Flip-Flops
 - iii. Decoders
- b. Create a 16-to-1 multiplexer by using only 4-to-1 Multiplexers. (Do not use any other gates)
- c. Simplify the following expressions by using suitable Multiplexer(s). (Use 8-to-1 or 16-to-1 multiplexers only)
 - i. $F = \bar{A}.\bar{B}.\bar{C} + A.\bar{B}.\bar{C} + \bar{A}.B.C + A.\bar{B}.C$
 - ii. $F = \bar{C}.\bar{D} + \bar{A}.\bar{C} + \bar{A}.\bar{D}$

Q3.

- a. Briefly describes the following terms (components).
 - i. 7-Segment displays
 - ii. Registers
- b. Draw a circuit diagram and a counter sequence for synchronous 4 bit up - counter. (use J-K Flip-flops)
- c. What are the differences between CMOS and TTL ICs?
- d. Draw an electronic circuit diagram for the following expression. (Use the given diagram sheet and attach it to your answer book)

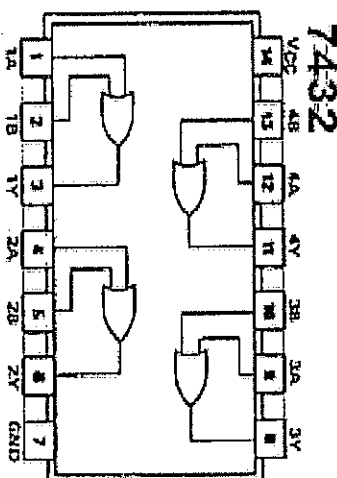
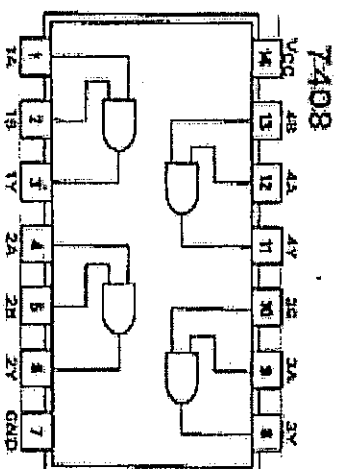
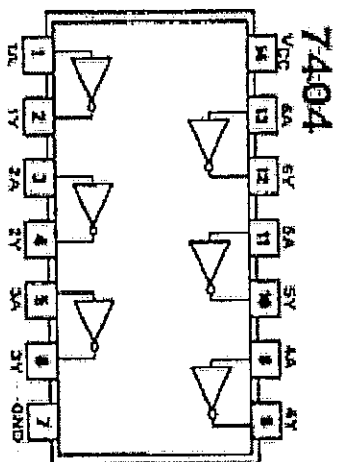
$$F = A.\bar{B} + A.\bar{C} + \bar{A}.D + C.D$$

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Index No:

5V +

out



- A ●
- B ●
- C ●
- D ●