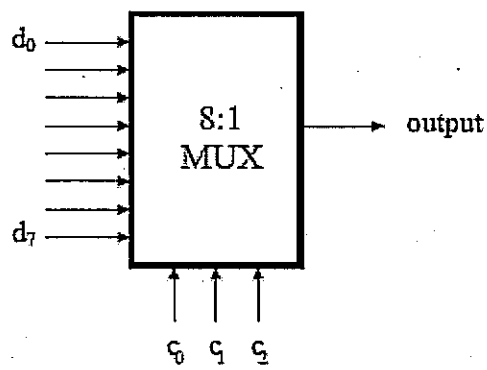
THE OPEN UNIVERSITY OF SRI LANKA
B.Sc DEGREE PROGRAMME: LEVEL 04
FINAL EXAMINATION: 2010/2011
CSU2178: DIGITAL COMPUTER FUNDAMENTALS
DURATION: **TWO HOURS** (2 HOURS)

Date: **12th July, 2011** Time: **9.30 a.m. – 11.30 a.m.**

Answer FOUR Questions ONLY.

1.

A multiplexer is a device that selects one of its inputs as the output. The selection is determined by a set of control signals. For example, in the 8:1 multiplexer shown below, the output will be equal to d6 when c2 = 1, c1 = 1 and c0 = 0.



1.1. Give a circuit which implements this 8:1 multiplexer using logic gates.

1.2. Using 8:1 multiplexers (and a 2:1 multiplexer, if needed), build a 16:1 multiplexer and draw it's circuit diagram.

1.3. Eight sensors each feed eight bits of information to a circuit which processes the information. It is decided that instead of using 64 signal lines, the data will be multiplexed onto eight data lines. Three address lines are used to indicate the sensor which uses the data line. The sensors will be continually cycled through in order.

a) A three-bit counter is required to cycle through the values for the address lines. Design such a counter. You may assume the availability of a clock signal.
b) An 8:1 multiplexer has eight data inputs, three control inputs and an output. The value of the control inputs determines the data input which is selected as the output. Design an 8:1 multiplexer (to implement the above mentioned logic).
c) Show how these components would be used to build the required system.
d) How would you modify the design if there were 256 sensors continually cycled through in order?

2.

2.1. Simplify the following expressions using Boolean algebra:

a) $X = (A + B + A.B).(A + B).A.B$

b) $Y = (A + B + A.B).C$

2.2. Given:

$$F = A.B.C.D + A.C + B.C.D + B.C + A.C.D + A.B.C.D$$

a) Show using a Karnaugh map that F can be simplified to;

$$F1 = A.B + A.B + A.C + B.C.D$$

b) Show that there are a total of four possible expressions for F.

c) Show how F1 can be implemented using NAND gates and draw the circuit diagram. Assume that complemented input variables are available.

d) Now implement F1 assuming that only 2-input NAND gates are available.

2.3. What is a ***don't care*** term and how can such terms arise in practice?

3.

3.1. In a particular computer system, numbers are represented using words having a length of 4 bits.

a) What is the range of positive numbers that can be represented using unsigned binary numbers?

b) Explain how the 2's complement representation can be used to describe signed binary numbers, using 4-bit words as an example.

c) Using decimal (base 10) representation for the answers, perform the following 2's complement 4-bit additions, noting any problems:

- 0110 + 1101
- 1010 + 1011

3.2.

a) Complete the following truth table that describes a single-bit full adder:
Where C_{IN} is carry-in, A and B are the input data, C_{OUT} is carry-out and sum is the SUM output. (Remember to write your answer on the answer script paper, i.e. not on the question paper.)

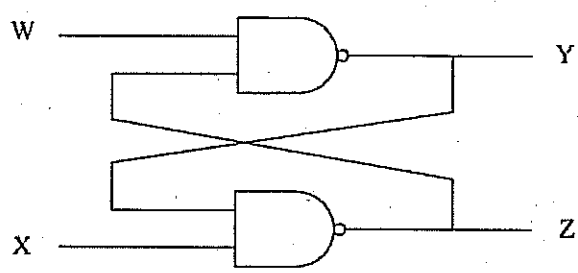
C_{IN}	A	B	C_{OUT}	SUM
0	0	0	0	
0	0	1	0	
0	1	0	0	
0	1	1	1	
1	0	0	0	
1	0	1	1	
1	1	0	1	
1	1	1	1	

b) Show how 4 single-bit full-adders can be combined to implement a 4-bit ripple carry-adder.

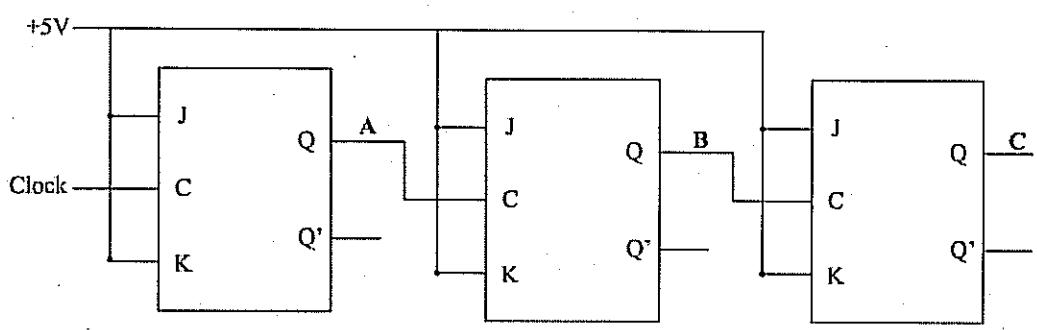
c) Show how C_{OUT} in part (a) can be implemented using only NAND gates.

4.

4.1. Explain the operation of the following circuit.



4.2. Consider the following Counter;



a) Draw the timing waveforms for the points A,B and C; assume that at t = 0 ; A,B,C=0

b) Based on your plots in the previous section, show that this circuit is a 3 bit counter. Explain which bit is the least significant bit and which is the most significant bit.

c) Show that the counter resets after the counting cycle is finished.

4.3. Explain the operation of an edge triggered D-type flip flop, taking care to explain any timing constraints.

5.

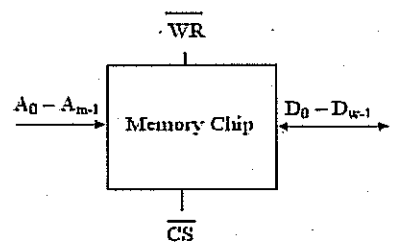
5.1. A compiler is a computer program that transforms programs written in a high level language such as C, Pascal into machine language. Explain the steps of the process of compiling a program refer as translation process.

5.2. Commercial Scalable Processor Architecture (SPARC) processor was developed at Sun Microsystems in 1980's. the style of architecture used in SPARC is known as RISC (Reduced Instruction Set Computer)

a) Name four types of instructions and give examples for each with the Mnemonic and the Meaning.
b) Write an Assembly language program to add two integers, where one integer is a constant (15) and the other is a positive integer in the Memory.
c) What are the usages of following addressing Modes?
   - Immediate addressing
   - Direct Addressing
   - Indirect Addressing

6.

6.1. RAM (Random Access Memory) ; Simplified pin out of a RAM chip is shown below;



a) What are the functions of each set of Pins on the above memory chip?
b) Design a RAM that stores Four Bit words. (Imagine RAM as a collection of registers)
c) Draw the simplified version of the four word by four bit RAM designed above.
d) How can you use Two four word by four bit RAMs in creating a four word by eight bit RAM (Use a diagram)?

6.2. A computer system may contain many components that need to communicate with each other. A bus is a common pathway that connects a number of devices. Describe what the parts of the bus and how the components communicate with each other.

6.3. Computer Systems have a wide range of communication tasks. Name three methods for managing inputs and outputs and describe two of them.