THE OPEN UNIVERSITY OF SRI LANKA
DEPARTMENT OF MATHEMATICS AND COMPUTER SCIENCE
B. SC. DEGREE PROGRAMME 2011/2012
FINAL EXAMINATION
CPU3141: DIGITAL COMPUTER FUNDAMENTALS
DURATION: TWO HOURS (2 HOURS)

Date: 13th June, 2012 **Time: 1.30 pm to 3.30 pm**

Answer **FOUR** Questions **ONLY.**

Q1.

a. Briefly explain the following terms.
   i. Binary Code
   ii. Unicode
b. Considering the *Signed Magnitude* of the negative binary integers, briefly explain how binary calculation is performed on the computer?
c. Use the *One's complement* method and compute the following binary values.
   i. 234 + 23 ii. (-234) + 123 iii. (-234) + (-345)
d. Briefly explain *Gray Code*.
e. Convert the following Gray Code into Binary.
   1001001

Q2.

a. What are *TTL* and *CMOS*?
b. Gate is an electronic device that can be made using transistors. Draw transistor based schematic diagram for the AND, OR and NOT gates.
c. Basic gates (NOT, AND, OR etc) can be modeled using NAND gates. Implement NOT, OR and AND gates through the NAND gate(s).
d. Consider the following truth table (A, B, C and D are inputs and X is the output).
   i. Write a logical expression for the above truth table (without minimization).
   ii. Minimize the expression using K-Map method.
   iii. Draw a circuit diagram using NOT, OR and AND gates.
   iv. Implement above circuit using NAND gates only.

A	B	C	D	X
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Q3.

a. What is a *combinational logic circuit*?

b. Draw truth table and the block diagram for the binary full adder.

c. The Multiplexer circuit is typically used to combine two or more inputs onto a single line.

   i. Draw a truth table and a block diagram for the two-input multiplexer.

   ii. Using two-input multiplexer, design an eight-input multiplexer.

d. Draw a truth table and a block diagram for the SR flip-flop.

e. Using SR flip-flop, implement the D flip flop.

Q4.

a. What are the differences between *Asynchronous* and *Synchronous* counters?

b. Draw a 4 bit Asynchronous Counter using JK flip flops.

c. Draw a timing diagram of the above circuit.

d. Briefly explain the how we can design an *Asynchronous Counter* as a *Frequency Divider*.

e. Using the Frequency Divider, draw a 125 kHz Counter by using 1MHz clock.

f. What are the disadvantages of the asynchronous counters?

Q5.

a. Briefly explain the following terms.
   i. Shift Registers.
   ii. Race Condition.
   iii. Circuit Hazards.

b. What are *Asynchronous Sequential Circuits*?

c. What is the design procedure of the asynchronous sequential circuits?

d. Draw a logic diagram using the primitive flow table given below. (Use the design procedure that has given as the answer for the above question (Q5-part c)).

State	Input (A)	Input(B)	Output
A	0	1	0
B	1	1	1
C	0	0	0
D	1	0	0
E	1	0	1
F	0	0	1

Q6.

a. Briefly describe the following terms.
   i. Memory hierarchy.
   ii. Programmable Logic Devices.
   iii. Memory organization of MSP430 family.

b. Using bus system and the CPU of the computer, explain how CPU works?

c. A single RAM cell can be implemented through the D type flip-flop. Draw a memory cell circuit with Write/Read and Data in/out.

d. What are the Interaction Policies for main memory?