The Open University of Sri lanka
B.Sc Degree Programme – Level 04
Department of Mathematics and Computer Science
Open Book Test 2011/2012
CSU2178 : Digital Computer Fundamentals

Duration:**One and Half hours only (1.5 hrs)**

Date:**01.03.2012** Time:**04.00 pm – 05.30 pm**

Answer ALL Questions.

Q1.

a. Prove the following rules by considering A, B and C as boolean parameters.
   i. Distributive Law
   ii. Associative Law
   iii. Commutative Law

b. Prove **DeMorgan's Theorem.**

c.
   i. Get the Boolean expression for the output of the following truth table.

Inputs			Output
C	**B**	**A**	**Y**
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

   ii. Minimize the expression for Y using Boolean rules. State the rules.
   iii. Draw the Logic circuit for Y.

d. Minimize the following truth table using **K-map** method.

Inputs				Output
D	**C**	**B**	**A**	**Y**
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0

1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Q2.

a. What are the functions of the following digital components?
   i. Multiplexer
   ii. Demultiplexer
   iii. Decoder
   iv. Encoder
b. Draw the **Block diagram** and **Circuit diagram** of 1 to 4 **Demultiplexer** where ; $F_0 = DA'B'$, $F_1 = DA'B$, $F_2 = DAB'$, $F_3 = DAB$
c. Describe the function of the **Multiplexer**.
d. Convert the following base 10 numbers into base 2.
   i. 27.25
   ii. 101.02
   iii. 302.222
e. Represent following numbers in **One's complement** and **Two's complement**. (Consider 8 bit represenatation)
   i. +15
   ii. -15
f. Draw the **Adder circuit** fot 3 bit binary addition opearion.

Q3.

a. What are the differences between **Sequential Logic** and **Combinational Logic**?
b. Draw the Block diagrams to represent Combinational Logic and Sequential Logic. Describe the function of both logics.
c. Briefly describe **Circuit Hazard** using an example circuit.
d. Draw the truth table for the output of **S-R Flip-Flop.**
e. Draw the Circuit diagram and Timing diagram for **Clocked S-R Flip Flop.**