THE OPEN UNIVERSITY OF SRI LANKA
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

FINAL EXAMINATION - 2013/2014

ECX6330 – ELECTRONIC SYSTEMS **(Closed Book)**

ANSWER ANY FIVE QUESTIONS.

Date 03.09.2014 ***Time: 9:30-12:30 hrs.***

Q1. Consider the circuit in the Figure-Q1.

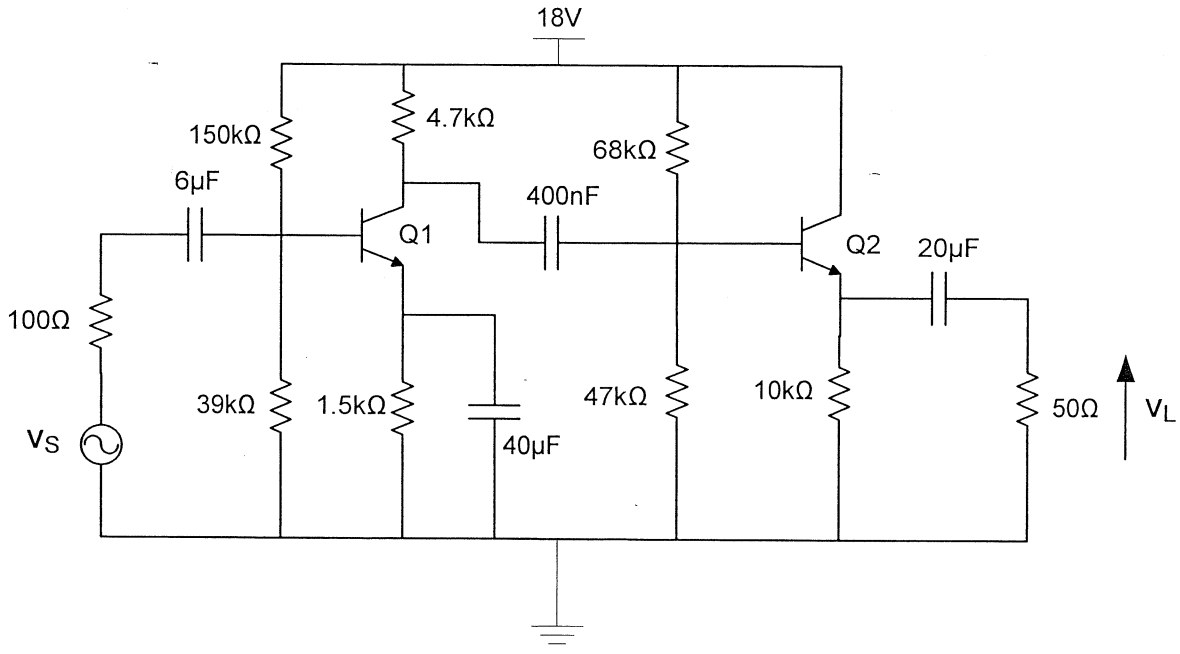

Figure-Q1

Q1: $h_{ie} = 1.4k\Omega, h_{re} = 2 \times 10^{-4}, h_{fe} = 180$
Q2: $h_{ic} = 2k\Omega, h_{rc} = 1, h_{fc} = -101$

(a) Draw the low frequency equivalent circuit. **(6 Marks)**

Hence find,

(b) Input impedance. **(6 Marks)**
(c) Output impedance. **(2 Marks)**
(d) Mid band voltage gain $\frac{V_L}{V_S}$. **(6 Marks)**

Q2. Let the transistor in the amplifier circuit in Figure-Q2 has the following parameters with the usual notation.

$g_m = 3.2mS, r_d = 100k\Omega, C_{gs} = 4pF, C_{ds} = 0.5pF$ and $C_{gd} = 1.2pF$.

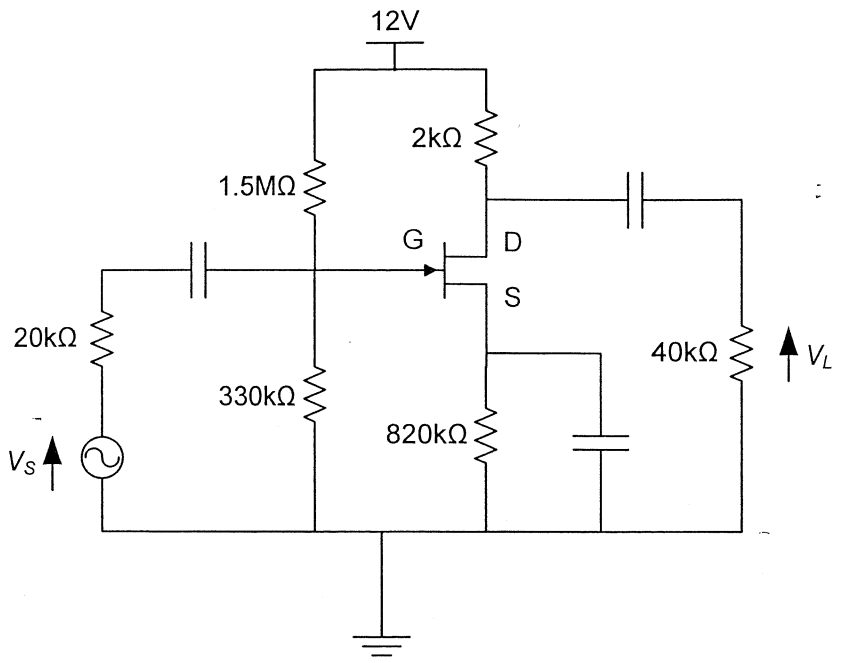

Figure-Q2

(a) Draw the high frequency equivalent circuit for this amplifier circuit. **(6 Marks)**

(b) Calculate the input and output impedances. **(8 Marks)**

(c) Hence, find the approximate upper cutoff frequency of this amplifier. **(6 Marks)**

Q3.

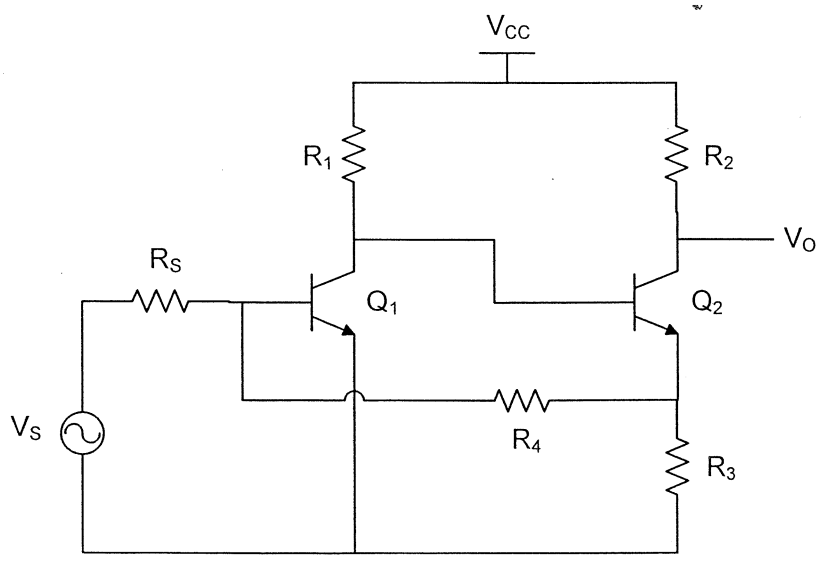

Figure-Q3

A feedback amplifier is shown in the above Figure-Q3. $R_1 = 3.3k\Omega$, $R_2 = 560\Omega$, $R_3 = 47\Omega$, $R_4 = 1.2\ k\Omega$, $R_s = 1k\Omega$, $h_{fe} = 50$, $h_{ie} = 1.2k\Omega$ and $h_{re} = h_{oe} = 0$.

(a) Identify the type of feedback used. **(2 Marks)**

(b) Using an equivalent circuit, calculate the current gain without the feedback. **(12 Marks)**

(c) Hence find voltage gain of this feedback amplifier. **(6 Marks)**

Q4. (a)

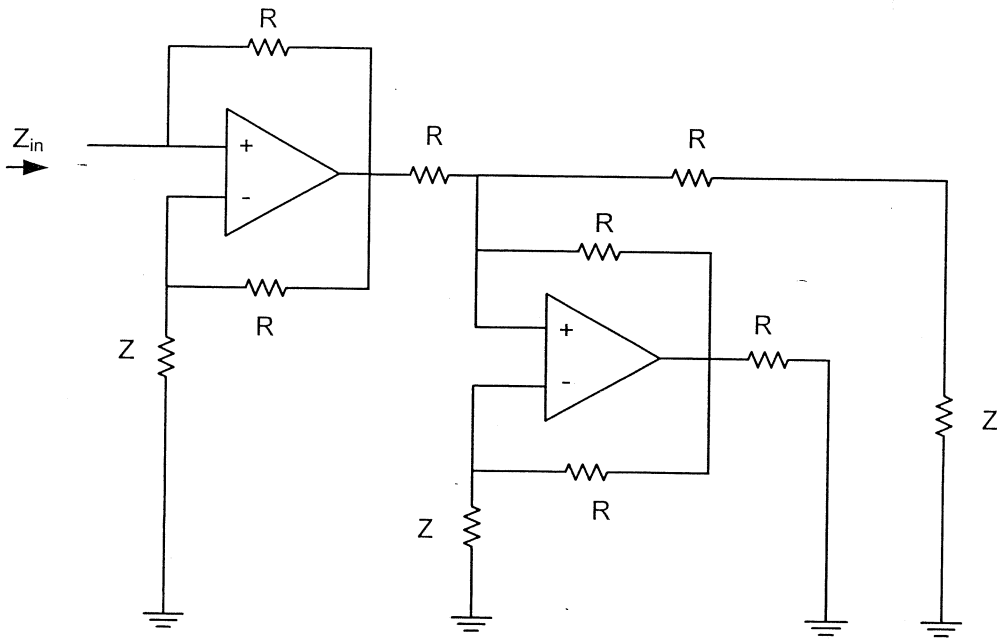

Figure –Q4 (a)

Show that the input impedance of the circuit in Figure-Q4 (a) is, $Z_{in} = \frac{R^2}{Z}$.

(**Hint**: Identify a common circuit segment including a single op-amp and find the input impedance of this segment) **(12 Marks)**

(b) Figure-Q4 (b) shows an operational amplifier application in a Schmitt trigger circuit. Find the lower and upper trigger levels. Hence draw the hysteresis loop. (Assume that the output switches between +15V and -15V) **(8 Marks)**

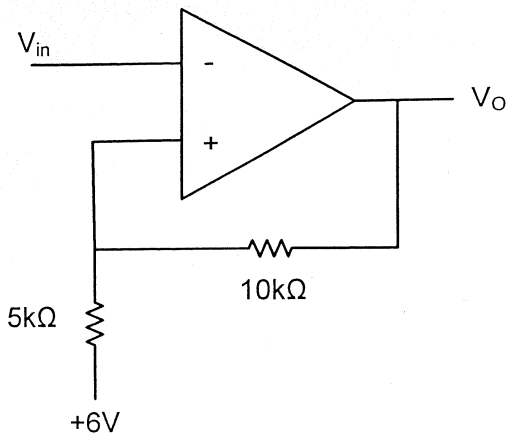

Figure –Q4(b)

Q5.

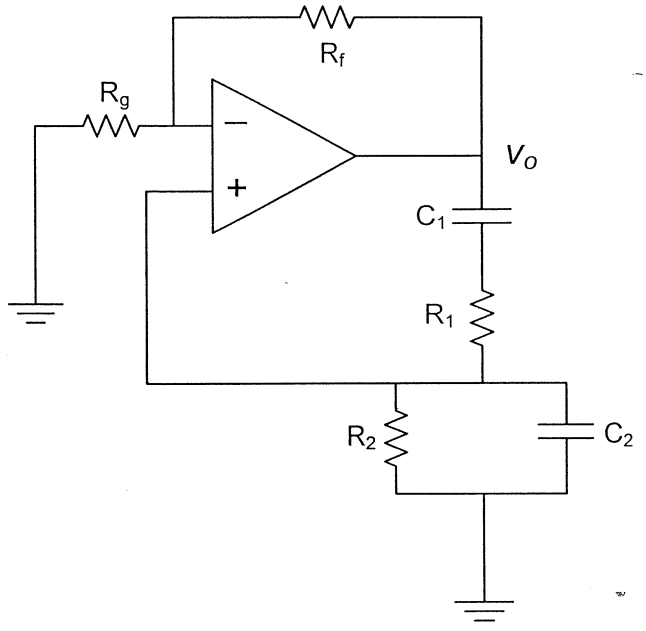

Figure-Q5

(a) Starting from the first principles, derive the Barkhousen criteria for oscillations to occur. **(4 Marks)**

(b) Stating all your assumptions, derive an expression for the feedback factor for the circuit in Figure- Q5. **(8 Marks)**

(c) Derive an expression for the forward gain. **(4 Marks)**

(d) Hence find the frequency of oscillation. **(4 Marks)**

Q6.

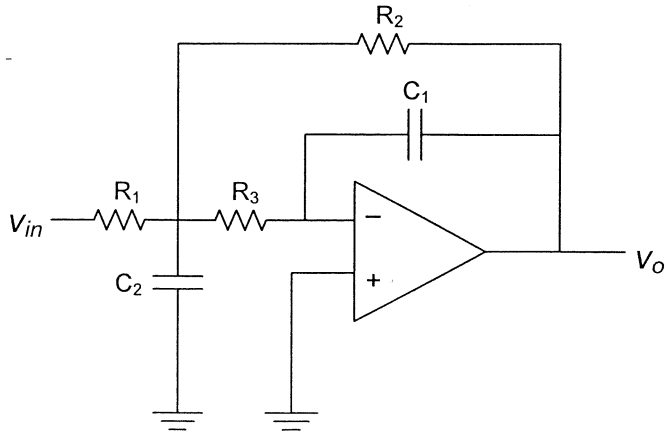

Figure-Q6

(a) List commonly used filter transfer functions and their characteristics. **(4 Marks)**

(b) Find the transfer function of the second order filter stage shown in Figure-Q6. **(8 Marks)**

(c) Use the circuit in Figure-Q6 and the other circuit components as necessary to design a 3rd order unity gain Butterworth low pass filter. State all the component values you select for the design.

Hint: First and second order transfer functions are of the forms $\frac{A_0}{1+a_1 s}$ and $\frac{A_0}{1+a_2 s+b_2 s^2}$ respectively.

(8 Marks)

Q7.

(a) Using suitable diagrams, explain the operation of a successive approximation type ADC. **(3 Marks)**

A certain successive approximation type 8 bit ADC can handle input voltages in the range $0 - 8V$. Find,

i. The resolution of the ADC. **(3 Marks)**

ii. The conversion speed of the ADC for a $1MHz$ clock. **(3 Marks)**

iii. Sketch the plot of DAC output voltage vs time for a conversion of $3.2V$. **(3 Marks)**

(b) Design and implement a 2 bit adder using a ROM.(Clearly show the design steps) **(4 Marks)**

(c) A certain logic circuit has four inputs A, B, C, D and two outputs Y_1 and Y_2.

$Y_1 = \sum(0,1,4,5,8,14,15)$,

$Y_2 = \sum(0,2,5,7,8,13,14,15) + \prod(6,10)$.

Simplify the functions and implement using a PLA. **(4 Marks)**

Q8.

(a) Differentiate the Mealy and Moore logic. **(4 Marks)**

(b) A 4 bit parallel binary multiplier for positive numbers is using the shift and add method. The system block diagram is shown in Figure-Q8.

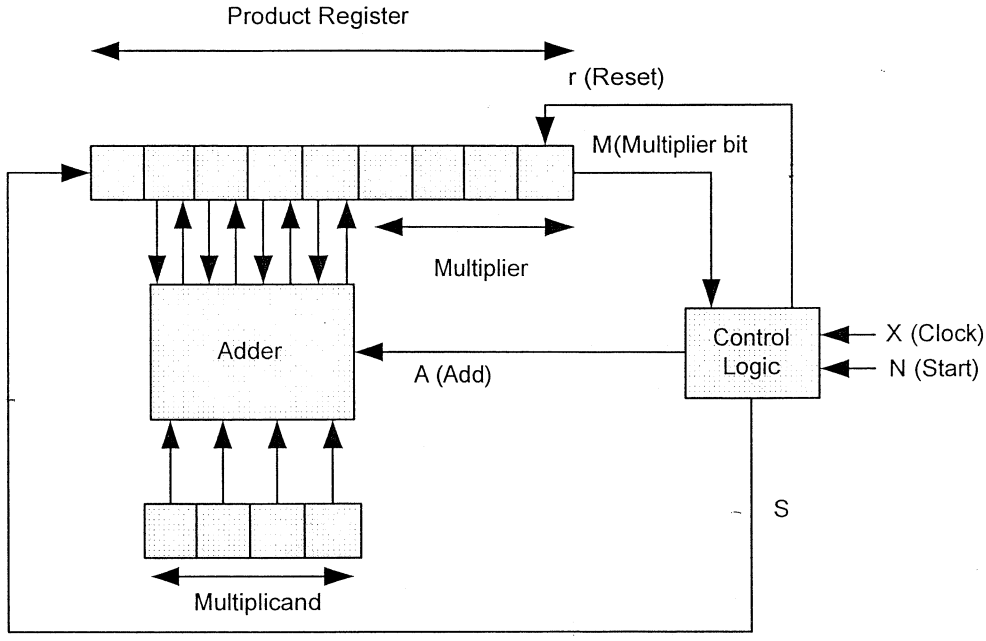

Figure -Q8

The multiplier is controlled from the box labeled "Control Logic". The inputs to the controller are the clock signal (X), the start signal (N) and the multiplier bit M. The outputs from the controller are the shift pulse (S), the add pulse(A) and the rest pulse (r). The control logic is to be designed such that if the multiplier bit , M is 1 at a given clock time, an addition takes place (otherwise not). The multiplier bit is then reset to 0 and the next clock time, a shift occurs. Using synchronous sequential circuit design technique,

i. Provide the state diagram for the control logic. **(6 Marks)**

ii. Provide a transition table. **(6 Marks)**

iii. Design the control logic for the multiplier. **(4 Marks)**