THE OPEN UNIVERSITY OF SRI LANKA
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
BACHELOR OF TECHNOLOGY
ECX5231 –NETWORK THEORY
FINAL EXAMINATION - 2014/2015
DURATION – 3 hrs.

CLOSED BOOK

Date: 19th September 2015 **Time: 09.30 - 12.30 hrs.**

Instructions:

This paper consists of seven (06) questions. Answer any four (4) questions. All questions carry equal marks

Q1. A cascaded connected two two-port networks which are described by y and h parameters are shown in figure Q1.

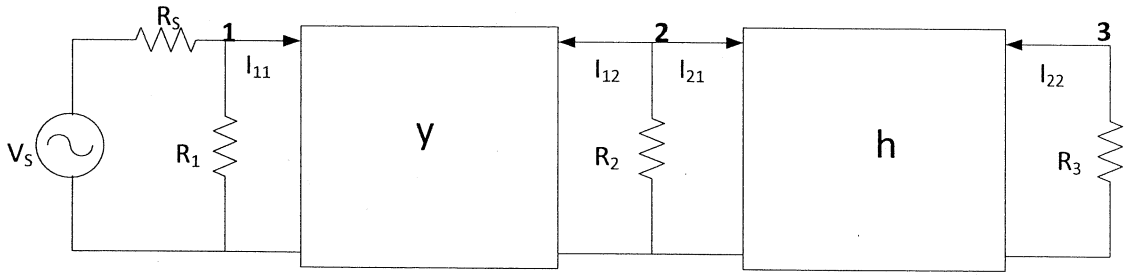

Figure Q1

Short circuit admittance (y) parameters

$I_{in} = y_{11} V_{in} + y_{12} V_{out}$

$I_{out} = y_{21} V_{in} + y_{22} V_{out}$

Inverse transmission (h) parameters

$V_{out} = h_{11} V_{in} - h_{12} I_{in}$

$I_{out} = h_{21} V_{in} - h22 I_{in}$

I. State unknown variables of the above circuit configuration shown in Figure Q1 [3]
II. Develop stamps for the two port elements "y" and " h" and all other elements shown in the figure Q1 [15]
III. Formulate the matrix equation for the circuit shown in figure Q1 with help of above developed stamps [7]

Q2. Every linear circuit has a set of parameters which fully described its behavior. For small ac signals, a transistor behaves like a linear device and transistor can be represented by characteristic set of h parameters. Figure Q2.1 shows a hybrid small signal model for common emitter configuration with emitter grounded while Figure Q2.2 shows an amplifier circuit connected in a common emitter configuration.

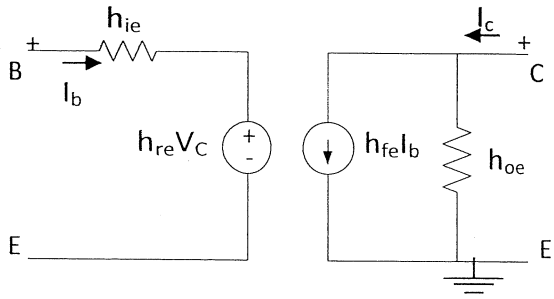

Figure Q2.1

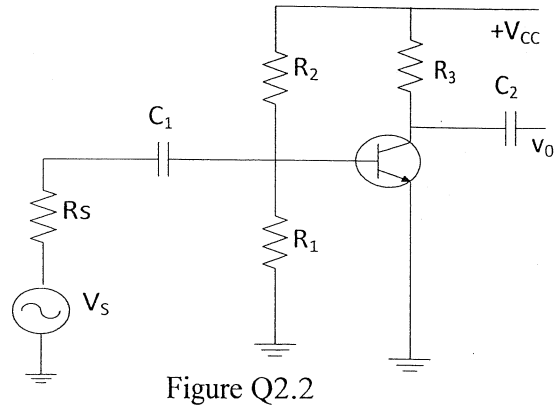

Figure Q2.2

I. Develop the circuit stamp for the transistor hybrid small signal model shown in Figure Q2.1 [5]

II. Draw the equivalent ac small signal circuit model for circuit shown in Figure Q2.2 with replacing the CE transistor by its hybrid circuit model [5]

III. Develop stamps for all the circuit elements in the equivalent circuit drawn in Q2. (II) [10]

IV. Formulate the matrix equation for the circuit shown in figure Q2.2 with help of above developed stamps [5]

Q3. A UJT relaxation oscillator, which generate voltage triggering pulse to the gate terminal of the SCR is shown in figure Q3.1. Equivalent circuit of the UJT is shown in the Figure Q3.2.

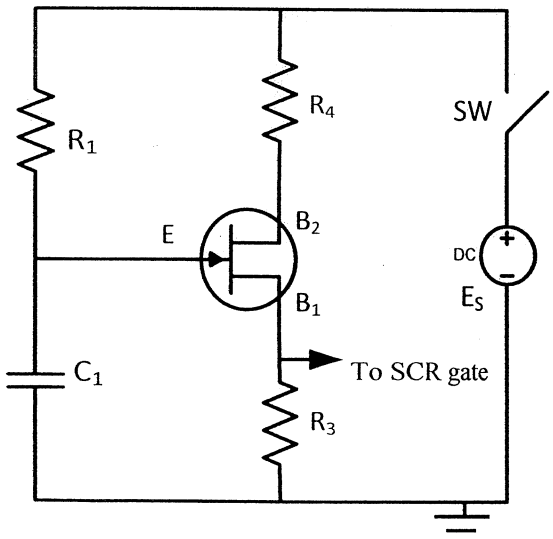

Figure Q3.1

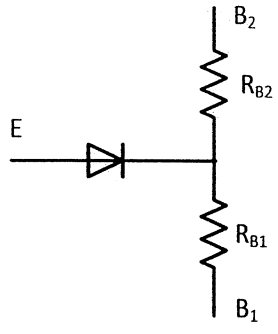

Figure Q3.2

Current Voltage relationship of the diode given as; $i(v) = I_S\,(e^{\frac{v}{v_t}} - 1)$
Where I_S is the reverse saturation current, V_t is the thermal voltage and V is the voltage between the diode.

Assuming the switch "SW" is closed at t=0, perform transient analysis for the circuit shown in Figure Q3.1 by following the steps given below; (capacitor is fully discharged)

I. Draw the simplified models of the circuit shown in Figure Q3.1 by replacing the UJT by its equivalent circuit. [2]
II. Develop circuit stamps of each circuit component and obtain the circuit equations in the format of Ex' + Gx + p (x) – w (t) = 0 [15]
III. Develop an algorithm by combining both Euler and Newton's methods to solve the above system of equations [3]
IV. Sketch flow chart to describe the simulation of transient analysis of the circuit. [5]

Q4. Transient analysis of an electrical circuit is a time domain analysis when the excitation of the circuit is switched from one stable state to another. Perform transient analysis for the circuit shown in Figure Q4 by following steps given below.

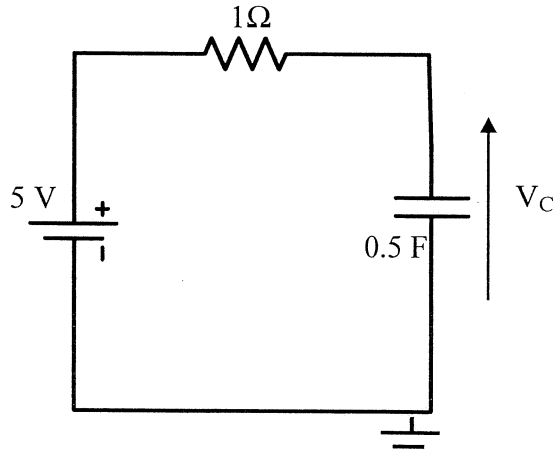

Figure Q4

I. Develop companion model for the capacitor of capacitance 0.5 F [4]
II. Draw the equivalent circuit using above companion models and write stamps for each element. [4]
III. Use stamps in part (b) to formulate the circuit to the format of [G] [X] = [I]. Where [G] is nodal admittance matrix. [4]
IV. Assuming initial voltage across the capacitor $V_C(0)$ =0, use the results obtained in part III to calculate the voltage across the capacitor V_C at t=0,0.5s,1s,1.5s (time step (h) is 0.5s) [10]
V. State how to ensure the solution has reached the final stable solution or steady state in a simulation program of transient analysis [3]

Q5.

a) State what the sensitivity analysis is and describe the importance of it in circuit analysis [3]

b) Develop the adjoint network model of the Current Controlled Voltage Source by using of Tellegens theorem [4]

c) A DC circuit having a Current Controlled Voltage Source is shown in Figure Q5.

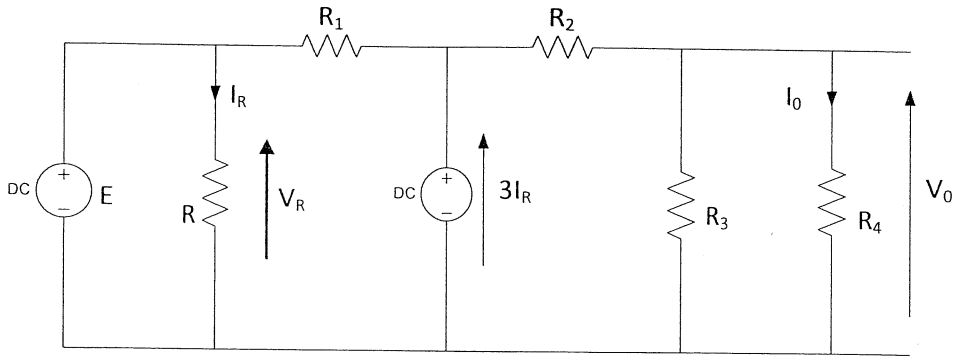

Figure Q5

I. Draw adjoint network models of the circuit shown in figure Q5, when the sensitivity interests is;

a) Output Voltage (V_0) [2]

b) Output current(I_0) [2]

II. Find out currents (I_R) and voltage (V_R) in the figure Q5 and through resistor R in the adjoint network model drawn under Q5.I.(a) [10]

III. Find the sensitivity of the output voltage (V0) with respect to the Resistor (R) [4]

Q6. A simple RLC circuit is shown in Figure Q6

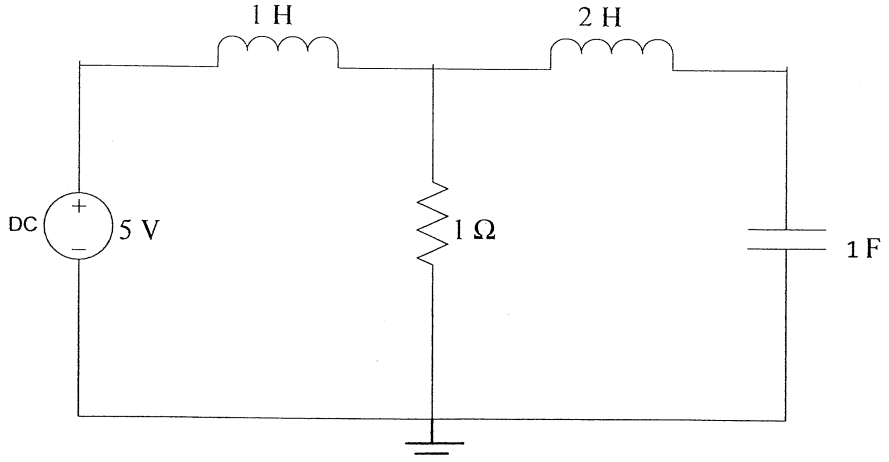

Figure Q6

I. State types of circuit analysis can be performed using state space analysis [5]
II. By selecting proper state variables, obtain the State Space equations for the circuit shown in figure Q6 [10]
III. Express above state space equations in its standard matrix form [3]
IV. If initial states of inductors are 0 and capacitors is 5V ,calculate the voltage across the capacitor and Current through 1Ω resistor at t= 0, and 1μs [7]