THE OPEN UNIVERSITY OF SRI LANKA
BACHELOR OF TECHNOLOGY - LEVEL 5
ECX5236 – COMPUTER ARCHITECTURE
FINAL EXAMINATION 2014

DURATION: THREE HOURS

DATE: 19th September 2015 **TIME: 09:30 – 12:30 HOURS**

Answer any ***five*** questions. All questions carry equal marks.

1.

(i) Comment on the following statement giving reasons.

"Hit ratio can be improved by using faster memory i.e. memory with less access time."

(ii) What is meant by loosely coupled multiprocessors and tightly coupled multiprocessors?

(iii) Describe the Flynn's classification (SISD, SIMD, MISD and MIMD) on computer organisation giving block diagrams for each organization

(iv) A transaction processing system is considered for a PC. The PC executes instructions at 100 MIPS and has a disk with a total mean access time of 20 ms. Four disk accesses and 100,000 instructions are needed for each transaction. How many transactions per second are possible with this system?

2.

(i) Describe the following addressing modes briefly: *register*, *absolute*, *immediate*, and *register indirect* modes.

(ii) In a source code a programmer declared an array of integers. All elements of the array are signed 16-bit integers. Your task is to hide a text in English using this integer array and all characters of the text are in extended ASCII codes (8 bits). An integer number represents two characters and they are written in consecutive bytes of the element.

(a) Show that after hiding a text in English the array contains only positive numbers.

(b) What will be decimal numbers of the array if you hide the text OUSL? The ASCII code of the each letter is 79, 85, 83 and 76 in decimal respectively.

(c) Draw a diagram to show how the given text is stored in the memory. Assume that the memory is byte addressable.

(d) Give an algorithm to retrieve the hidden text from the memory.

3.

(i) Describe the two types of data rate: *media data rate* and *interface data rate*.

(ii) Consider specifications of a typical disk as follows. The advertised average seek time is 9ms, the transfer rate is 4MB/s, rotates at 7200 rpm, and the controller overhead is 1ms. Assume the disk is idle so that there is no queuing delay.

(a) What is the average time to read or write a 512-byte sector?

(b) If the measured seek time is 33% of the calculated average, what is the average time to read or write a 512-byte sector?

(iii) Briefly describe three methods which improve the average disk accessing time.

4. An enhancement in a computer system improves only some part of the system. Accordingly improvement of the performance depends on the impact of the enhanced part. The f denotes the fraction of the computation time in the old system that can be improved with the enhancement made; S_e is the achievable speedup only if the enhanced part of the system is used.

(i) If the old time of the system (without improvement) is T_{old} formulate the new time T_{new} of the system after the enhancement.

(ii) The speedup of the new system (after the improvement) is

$$S_{new} = \frac{T_{old}}{T_{new}}.$$

Accordingly derive an equation for S_{new} in terms of f, S_e, which is Amdahl's law.

(iii) The MIPS rating of a processor is 1000. However the processor requires at least one memory access per instruction. The memory latency of the system is 10 ns. If you are able to double the MIPS rating of the processor what is the achievable overall speedup of the system. Assume that there is no change in memory latency. You have to show how the Amdahl's law can be used for solving the problem.

5. Two computers are connected each other through their COM2 serial ports. These ports are operating at 9600bps and are based on 8250 family UARTs.

(i) Give a flowchart of a subroutine that transmits an ASCII character (7 bits) using odd parity, 1 start bit, and 2 stop bits. Clearly state all values of port registers and their addresses wherever they are used. For necessary port register description refer the appendix.

(ii) Show how you use the above subroutine to send a file (all character codes are less than 127) to the other computer.

(iii) Estimate the minimum transmission time if the file is n Kbytes in size.

(iv) How do you set up connections of two parallel ports of the computers if you want to send a file through these ports? Briefly describe the process of transmitting files.

6.

(i) Throughput of a pipeline is inversely proportional to the bottleneck of the pipeline. Explain the statement.

(ii) Consider a four–segment normalized floating-point adder (Fig. 1) with a 10 ns delay per each segment, which equals the pipeline clock period.

(a) Name the appropriate functions to be performed by the four segments according to the floating-point addition.

(b) Using the given pipeline adder (Fig. 1) draw a block diagram of a architecture to add 100 floating-point numbers $A_1+A_2+\ldots+A_{100}$, assuming that the output Z of

segment S_4 (Fig.1) can be routed back to any of the two inputs X or Y of the pipeline with delays equal to any multiples of the period.

(c) Find the minimum time required to add all 100 numbers.

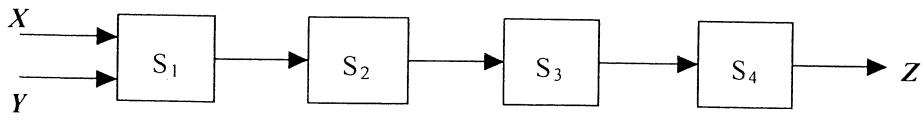
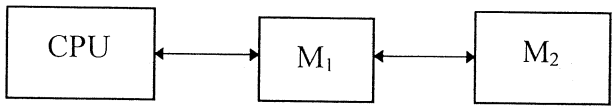


Fig. 1

7.

(i) Consider two-level memory hierarchy (M_1, M_2) for a computer system, as depicted in the following diagram.



Let C_1 and C_2 be the costs per bit, S_1 and S_2 be the storage capacities, and t_1 and t_2 be the access times of the memories M_1 and M_2, respectively. The hit ratio H is defined as the probability that a logical address generated by the CPU refers to information stored in the memory M_1.

(a) What is the average cost C per bit of the entire memory hierarchy?

(b) Under what condition will the average cost per bit C approach C_2?

(c) What is the average access time t_a for the CPU to access a word from the memory system?

(d) Let $r = t_2 / t_1$ be the speed ratio of the two memories. Let $E = t_1 / t_a$ be the access efficiency of the memory system. Express E in terms of r and H.

(e) If the speed ratio of the two memories is 100, what is the required minimum value of the hit ratio to make the access efficiency of the memory system over 0.90?

8.

(i) Name three organizations of cache memory and describe them briefly.

(ii) Briefly describe the tasks of an I/O system of a computer.

(iii) Write policies are needed for data caches when an instruction writes data to the cache. Briefly describe the Write Back and Write Through policies.

(iv) A colour display has maximum resolution of 640x480 pixels. It displays 256 different colours simultaneously. The display should be refreshed normally at the rate of 60 times per second.

(a) How many bits does it need to save information of colours per pixel?

(b) What is the minimum size of the display buffer memory?

(c) What would be the data rate that the display works properly?

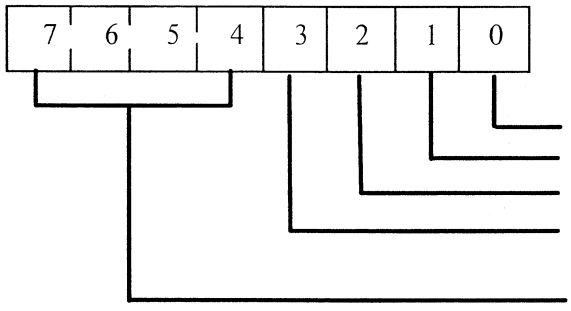
Appendix

8250 Family Register Definitions

Register Name	Offset	Abbreviation	Access Type
Receiver Buffer Register	0	RBR	Read Only
Transmit Holding Register	0	THR	Write Only
Interrupt Enable Register	1	IER	Read/Write
Interrupt Identification Register	2	IIR	Read Only
FIFO Control Register (16550)	2	FCR	Write Only
Line Control Register	3	LCR	Read/Write
Modem Control Register	4	MCR	Read/Write
Line Status Register	5	LSR	Read Only
Modem Status Register	6	MSR	Read Only
Divisor Latch (16 bits)	0/1	DL	Read/Write

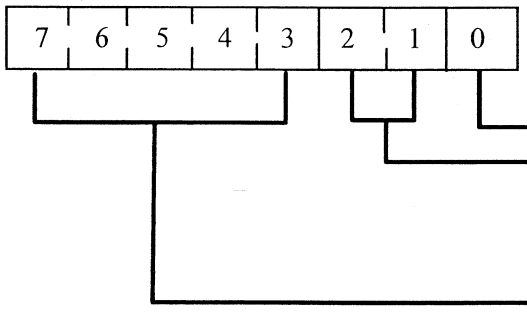
Base address of COM1 - 3F8h Base address of COM2 - 2F8h

IER



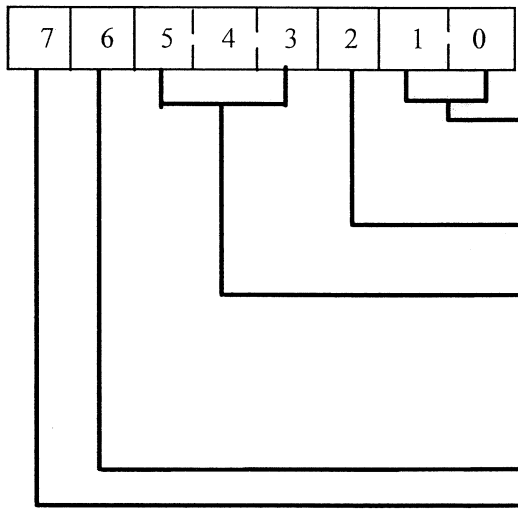
1- Received Data Available
1- Transmit Holding Register Empty
1 - Line Status
1 - Modem status (CTS, DSR, DCD or RI changes state)
Not used (= 0)

IIR



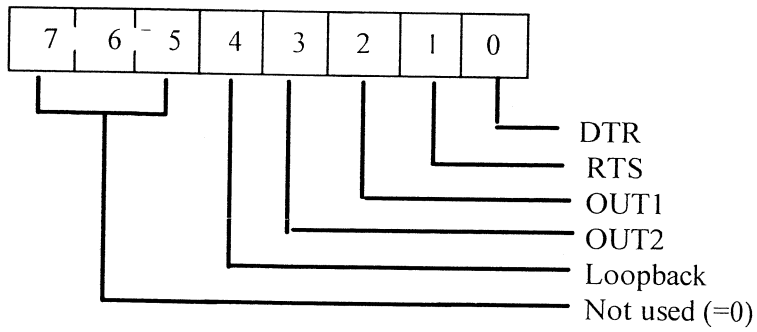
1 - No interrupt Rending
00 - Modem Status Interrupt
01 - Transmit Holding Register Empty
10 - Received Data Available
11 - Line Status
Not used (= 0)

LCR

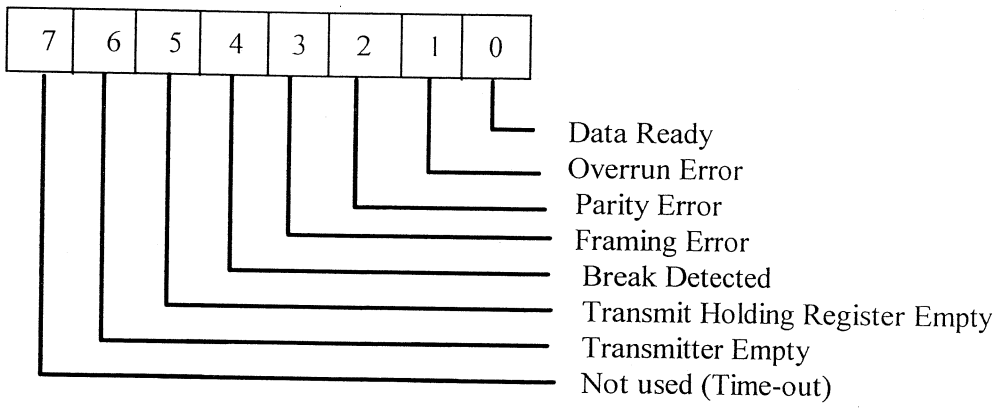


Word length Select
00 - 5 bits 10 - 7 bits
01 - 6 bits 11 - 8 bits
Number of Stop Bits
0 - 1 bit 1 - 2 bits
Control Bits
000 - No parity 100 - No Parity
001 - Odd Parity 101 - Mark Parity
010 - No Parity 110 - No Parity
011 - Even Parity 111 - Space Parity
Break Control
Divisor Latch Access Bit
1- Divisor Latch
0 - as usual RBR/ THR and IER

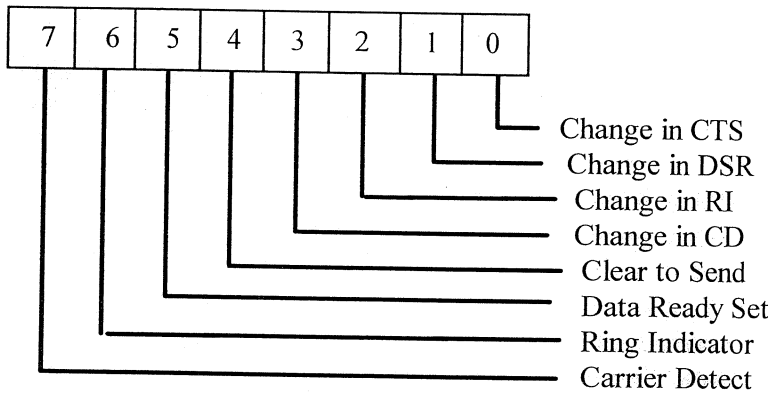
MCR


7
6
5
4
3
2
1
0
DTR
RTS
OUT1
OUT2
Loopback
Not used (=0)

LSR


7
6
5
4
3
2
1
0
Data Ready
Overrun Error
Parity Error
Framing Error
Break Detected
Transmit Holding Register Empty
Transmitter Empty
Not used (Time-out)

MSR


7
6
5
4
3
2
1
0
Change in CTS
Change in DSR
Change in RI
Change in CD
Clear to Send
Data Ready Set
Ring Indicator
Carrier Detect

Appendix A

Parallel port connector description

Pin: D-sub	Signal	Function	Source	Register		Inverted at con-nector?	Pin: Centron-ics
				Name	Bit #		
1	nStrobe	Strobe D0-D7	PC[1]	Control	0	Y	1
2	D0	Data Bit 0	PC[2]	Data	0	N	2
3	D1	Data Bit 1	PC[2]	Data	1	N	3
4	D2	Data Bit 2	PC[2]	Data	2	N	4
5	D3	Data Bit 3	PC[2]	Data	3	N	5
6	D4	Data Bit 4	PC[2]	Data	4	N	6
7	D5	Data Bit 5	PC[2]	Data	5	N	7
8	D6	Data Bit 6	PC[2]	Data	6	N	8
9	D7	Data Bit 7	PC[2]	Data	7	N	9
10	nAck	Acknowledge (may trigger interrupt)	Printer	Status	6	N	10
11	Busy	Printer busy	Printer	Status	7	Y	11
12	PaperEnd	Paper end, empty (out of paper)	Printer	Status	5	N	12
13	Select	Printer selected (on line)	Printer	Status	4	N	13
14	nAutoLF	Generate automatic line feeds after carriage returns	PC[1]	Control	1	Y	14
15	nError (nFault)	Error	Printer	Status	3	N	32
16	nInit	Initialize printer (Reset)	PC[1]	Control	2	N	31
17	nSelectIn	Select printer (Place on line)	PC[1]	Control	3	Y	36
18	Gnd	Ground return for nStrobe, D0					19,20
19	Gnd	Ground return for D1, D2					21,22
20	Gnd	Ground return for D3, D4					23,24
21	Gnd	Ground return for D5, D6					25,26
22	Gnd	Ground return for D7, nAck					27,28
23	Gnd	Ground return for nSelectIn					33
24	Gnd	Ground return for Busy					29
25	Gnd	Ground return for nInit					30
	Chassis	Chassis ground					17
	NC	No connection					15,18,34
	NC	Signal ground					16
	NC	+5V	Printer				35

[1]Setting this bit high allows it to be used as an input (SPP only)

[2]Some Data ports are bidirectional.

Parallel port register definitions

Base address: 0378h

Data Register (Base Address)					
Bit	***Pin: D-sub***	**Signal Name**	**Source**	**Inverted at connector?**	**Pin: Centronics**
0	2	Data bit 0	PC	no	2
1	3	Data bit 1	PC	no	3
2	4	Data bit 2	PC	no	4
3	5	Data bit 3	PC	no	5
4	6	Data bit 4	PC	no	6
5	7	Data bit 5	PC	no	7
6	8	Data bit 6	PC	no	8
7	9	Data bit 7	PC	no	9
Some Data ports are bidirectional. (See Control register, bit 5 below.)					
Status Register (Base Address +1)					
Bit	***Pin: D-sub***	**Signal Name**	**Source**	**Inverted at connector?**	**Pin: Centronics**
3	15	nError (nFault)	Peripheral	no	32
4	13	Select	Peripheral	no	13
5	12	PaperEnd	Peripheral	no	12
6	10	nAck	Peripheral	no	10
7	11	Busy	Peripheral	yes	11
Additional bits not available at the connector: 0: may indicate timeout (1=timeout). 1, 2: unused					
Control Register (Base Address +2)					
Bit	***Pin: D-sub***	**Signal Name**	**Source**	**Inverted at connector?**	**Pin: Centronics**
0	1	nStrobe	PC[1]	yes	1
1	14	nAutoLF	PC[1]	yes	14
2	16	nInit	PC[1]	no	31
3	17	nSelectIn	PC[1]	yes	36
[1]When high, PC can read external input (SPP only). Additional bits not available at the connector: 4: Interrupt enable. 1=IRQs pass from *nAck* to system's interrupt controller. 0=IRQs do not pass to interrupt controller. 5: Direction control for bidirectional Data ports. 0=outputs enabled. 1=outputs disabled; Data port can read external logic voltages. 6,7: unused					