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The Open University of Sri Lanka
Faculty of Engineering Technology
Department of Electrical & Computer Engineering

Study Programme	: Bachelor of Technology Honours in Engineering
Name of the Examination	: Final Examination
Course Code and Title	**: EEX4350 / ECX4150 Electronics II**
Academic Year	: 2017/18
Date	: 14th January 2019
Time	: 13.30-16.30hrs
Duration	: **3 hours**

General Instructions

1. Read all instructions carefully before answering the questions.
2. This question paper consists of **Eight (8)** questions in **Five (5)** pages.
3. Answer any **Five (5)** questions only. All questions carry equal marks.
4. Answer for each question should commence from a new page.
5. Relevant charts/ codes are provided.
6. This is a Closed Book Test (CBT).
7. Answers should be in clear hand writing.
8. Do not use Red colour pens.

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Q1. An impendence matching circuit is shown in Figure-Q1, where the transistor is having h_{ib} and h_{fb} 25Ω and 0.99 respectively. Neglect the effect of h_{rb} and h_{ob}.

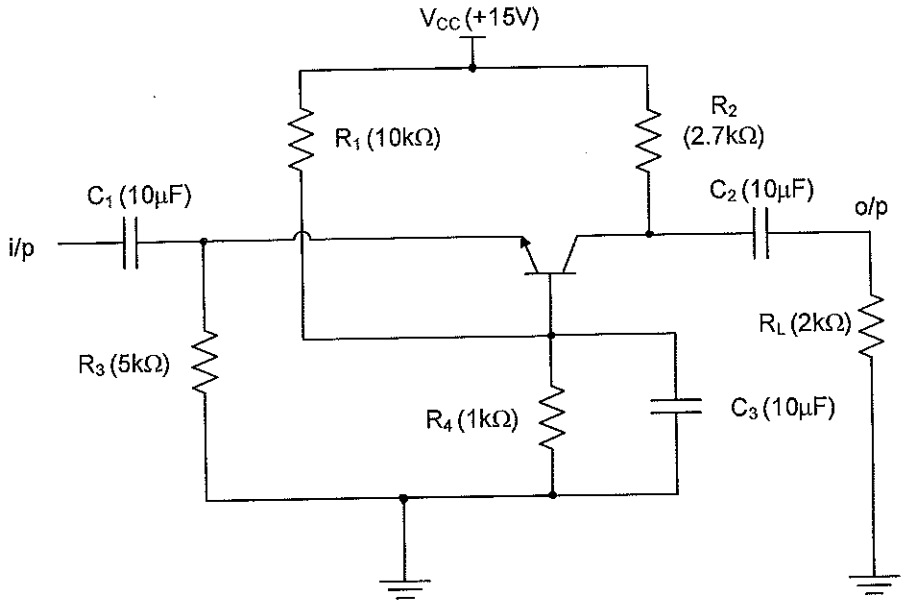

Figure-Q1

(a) Draw the low frequency hybrid parameter equivalent circuit. **(6 Marks)**

(b) Calculate the following.

i. Voltage gain. **(4 Marks)**
ii. Current gain. **(4 Marks)**
iii. Input impedance. **(3 Marks)**
iv. Output impedance. **(3 Marks)**

Q2.

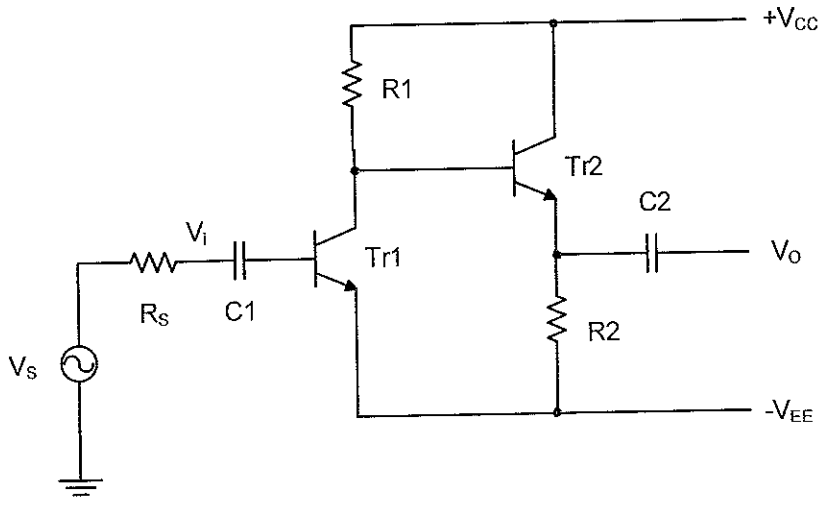

Figure –Q2

Consider the cascading amplifier setup in the circuit diagram shown in Figure-Q2, where Tr1 and Tr2 are identical.

Here,

$R_s = 1k\Omega,\ R1 = R2 = 5k\Omega, h_{ie} = 2k\Omega,\ h_{fe} = 50, h_{re} = 6 \times 10^{-4}, h_{oe} = 25\mu A/V,$

$h_{ic} = 2k\Omega,\ h_{fc} = -51, h_{rc} = 1, h_{oc} = 25\mu A/V.$

(a) Draw the low-frequency equivalent circuit using the h-parameter model of the transistors.
(You may assume the effect of some parameters to be negligible. Clearly state all your assumptions made) **(8 Marks)**

(b) Write down three equations to depict the relationships between base currents of the two transistors, V_s and V_o. **(3x2 Marks)**

(c) Hence calculate $\frac{V_0}{V_s}$. **(6 Marks)**

Q3.

(a) Compare class A, B, C and D power amplifiers in terms of their efficiency and output distortion. **(8 Marks)**

(b) A complementary push-pull class-B power amplifier is to be designed to deliver an average power of $16W$ to a 8Ω load. The power supply voltage V_{CC} is to be $5V$ greater than the peak output voltage.

i. Compute the average power drawn from the supply. **(4 Marks)**

ii. Compute the power conversion efficiency of the amplifier. **(3 Marks)**

iii. Determine the maximum power each transistor should be able to dissipate. **(3 Marks)**

iv. Why is the supply voltage selected 5V greater than the peak output voltage? **(2 Marks)**

Q4.

(a) Describe the operation of the SCR, DIAC and TRIAC with the help of their I-V characteristic curves. **(4 Marks)**

(b) Explain how half wave power control can be obtained using a TRIAC. **(4 Marks)**

(c)

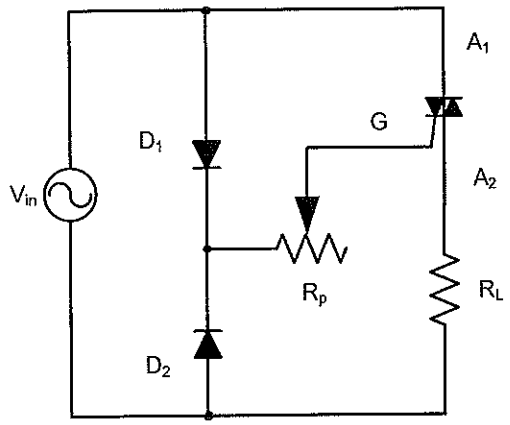

Figure-Q4

In the circuit shown in Figure-Q4, $v_{in} = 60V$ rms and $R_L = 15\Omega$. Let the rms load current be given by $I_{rms} = \frac{I_P}{\sqrt{2}}\sqrt{\left(1 - \frac{\theta}{180}\right) + \left(\frac{\sin 2\theta}{2\pi}\right)}$, where I_p is the peak load current and θ is the firing angle. Neglecting the drop across the TRIAC, calculate,

i. the maximum possible power that can be delivered to the load while conducting; **(6 Marks)**

ii. the maximum percentage load power delivered when the conduction angle is 45^0. **(6 Marks)**

Q5.

(a) List three characteristics of a practical operational amplifier and compare them with the ideal approximations. **(6 Marks)**

(b) Consider the circuit arrangement in Figure-Q5 (b). Show that $V_0 = \frac{R_2}{R_1}(V_2 - V_1)$ if $\frac{R_2}{R_1} = \frac{R_4}{R_3}$. **(6 Marks)**

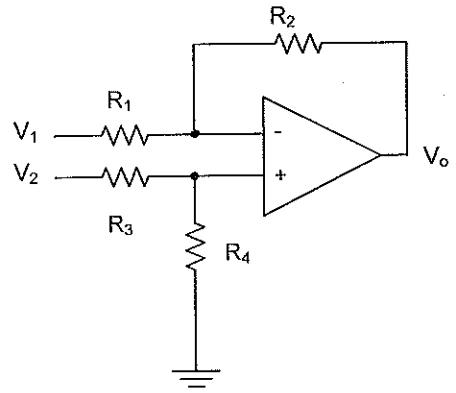

Figure-Q5 (b)

(c)

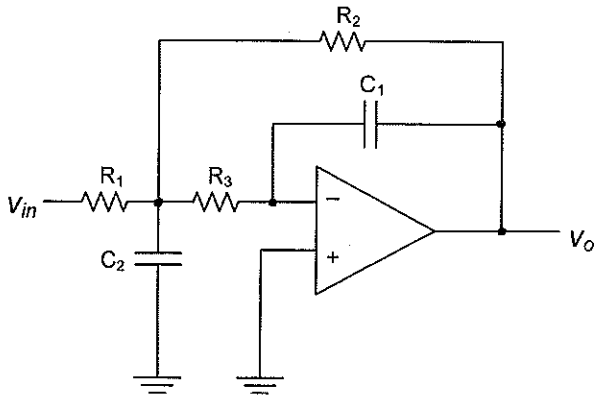

Figure-Q5 (c)

Derive the transfer function for the circuit in Figure Q5 (c) in terms of the frequency of the input signal. **(8 Marks)**

Q6.

(a) Draw the truth table and derive the Boolean expression for the sum and carry outputs in a single bit full adder. [You should clearly show the steps including the truth table and minimization]

(5 Marks)

(b) Carry-look-ahead adder is a concept used in modern microprocessor ALUs to generate all carry bits required in adding two multi bit numbers using a combinational circuit. This eliminates the need for long waiting in order to receive the rippled carry bits. Let $A = a_4a_3a_2a_1$ and $B = b_4b_3b_2b_1$ are two 4 bit numbers for addition. Consider the addition of a single bit position with a full adder.

i. Using the results of Q6 (a), show that the Boolean expression for the carry at the n-th bit ($n = \{1,2,3,4\}$) can be expressed in the form $C_n = G_n + C_{n-1}P_n$ where G_n and P_n are Boolean functions of $a_n$and b_n.

(5 Marks)

ii. Hence show that C_n can be expressed interms of c_0, a_n and b_n only ($n = \{1,2,3,4\}$). **(5 Marks)**

iii. Draw the complete carry generation combinational logic circuit with standard logic gates. **(5 Marks)**

Q7. A line following robot has to be designed with the following specifications.

- Robot has four sensors in a fixed linear array with the spacing between the sensors such that at most 2 sensors will be on the line at a time. On the other hand, there can be instances with a minimum of only one outer sensor on the line.
- Whenever the two center sensors are on the line, the robot should be moved forward; otherwise turning should be carried out to align the robot with the line. When the robot meets end of the line it should stop.
- Robot has two independent motors (connected to wheels) to generate motion.
  - Both motors on→ Forward motion
  - Left motor on, right motor off → Right turn
  - Left motor off, right motor on→ Left turn
  - Both motors off→ No motion.

A digital combinational control circuit takes the sensor outputs' logical values as inputs and outputs logic signals to the motors.

(a) Define the different inputs and outputs with suitable logic values. Hence, draw the truth table. **(10 Marks)**
(b) Derive the simplified logic expressions using Karnaugh maps. **(8 Marks)**
(c) Implement the circuit using common logic gates. **(2 Marks)**

Q8. Design a synchronous up-counter to produce the output sequence 0, 3, 6, 9, 12, 15, 0 ,... using J-K flip flops. Clearly show the following design steps in your design.

(a) State diagram. **(2 Marks)**
(b) State transition table. **(6 Marks)**
(c) Karnaugh map simplification of Boolean expressions. **(6 Marks)**
(d) J-K flip flop based logic circuit diagram. **(6 Marks)**