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The Open University of Sri Lanka
Faculty of Engineering Technology
Department of Electrical & Computer Engineering

Study Programme	: Bachelor of Technology Honours in Engineering
Name of the Examination	: Final Examination
Course Code and Title	**: EEX4530 Fault Diagnosis in Electronic Circuits** / ECX4230
Academic Year	: 2017/18
Date	: 18th January 2019
Time	: 0930-1230hrs

General Instructions

1. Read all instructions carefully before answering the questions.
2. This question paper consists of Eight **(8)** questions in **Eight (08)** pages.
3. Answer any **Five (5)** questions only. All questions carry equal marks.
4. Answer for each question should commence from a new page.
5. This is a Closed Book Test (CBT).
6. Answers should be in clear hand writing.
7. **Do not** use Red colour pen.

1. A single stage amplifier circuit is shown in figure 1. I_{DSS} =10mA, and $V_{gs(off)}$ = -3V.

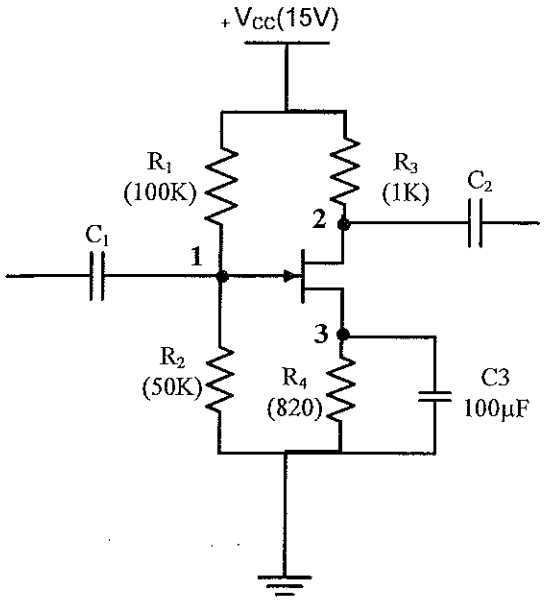

Figure 1

a. Calculate,
   i. Gate voltage [02 Marks]
   ii. Drain current [02 Marks]
   iii. Gate source voltage [02 Marks]
b. Calculate the test point voltages at no signal. [08 Marks]
c. Find the type of the fault with the faulty component/s in each case giving reason. [06 Marks]

Case	T.P 1(V)	T.P 2(V)	T.P 3(V)	Output
A	5	7.91	5.81	Low gain
B	5	15	0	No output
C	5	7.91	5.81	No output

2. A transistor amplifier is shown in figure 2.

The drain current of the transistor Tr1 is given by $I_D = 0.3(V_{GS} - V_P)^2$, where I_D is in mA, V_{GS} is in volts and $V_P = -4V$. You may assume usual notation. The current gain of the transistor Tr2 can be considered as high.

a. Calculate the current I_F and then find out the voltages at the test points when no signal is applied. **Do not assume** maximum swing at the output. [08 Marks]
b. Find out the amplitude of the input signal that will produce an output amplitude of 1V at 1 kHz. What is the phase relationship between the input and the output? [04 Marks]

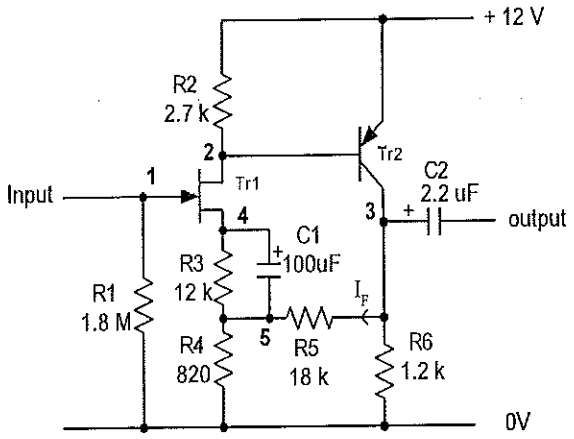

Figure 2

c. The test point voltages under fault conditions are shown in the following table. Identify the faulty component/s and fault type with reasons. [08 Marks]

Case	1	2	3	4	5	Output response
A	0	11.40	6.000	0.270	0.261	No output
B	0	11.40	11.80	3.139	0.201	Output clipped
C	0	11.40	0.012	3.077	0.197	No output
D	0	12.00	0	0	0	No output

3.

a. Draw a block diagram of an oscillator circuit. You should clearly show all the sub modules in your answer. [04 Marks]

b. The circuit of a Wien bridge oscillator producing sine wave output is shown in figure 3. All transistors are high gain, and RT is a thermistor.

i. Identify the components, which determines the output frequency. [01 Marks]

ii. What is the phase relationship of the signal at test point 5, with the signal at the base of Tr1? Also state the function of RT. [02 Marks]

iii. Estimate the frequency range of this oscillator. [02 Mark]

iv. Calculate the DC voltages at test points. [03 Marks]

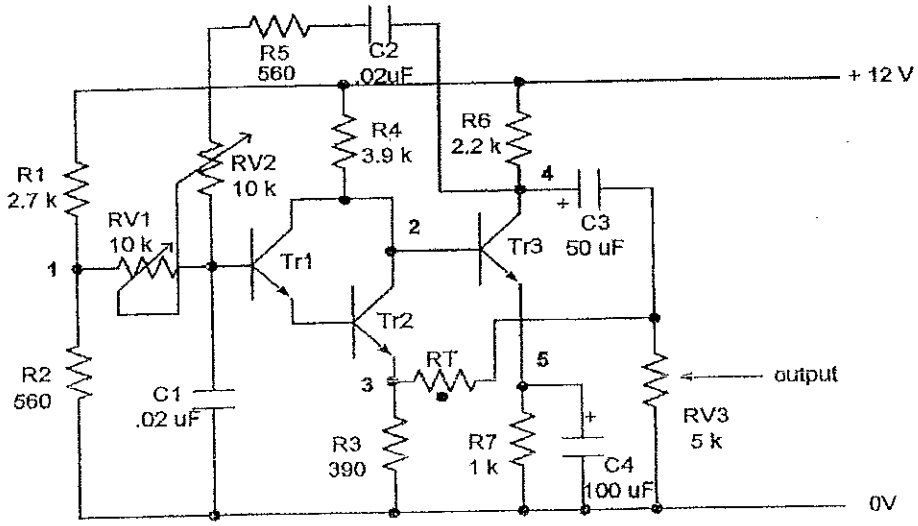

Figure 3

v. Following table shows the DC voltages at test points, under faulty conditions. Identify the faulty components indicating the relevant reasons. [08 Marks]

Fault	1	2	3	4	5	output
A	1.9	0	9.5	8.9	9.0	No output
B	1.9	0.7	6.7	6.5	15.0	No output
C	0	0	9.5	8.9	9.0	No output
D	1.9	0.7	6.6	6.0	10.9	Square wave

4. A Schmitt trigger circuit, used in a signal processing system is shown in figure 4 (a).

a. Calculate the input threshold voltages of this circuit. Find the test point voltages when the input is given 4V and 1V respectively. [06 Marks]
b. What is the hysteresis of this circuit? [02 Marks]
c. The shown in figure 4 (b) is given as an input to the circuit. Sketch the output waveform, clearly showing voltage and time values. [04 Marks]
d. Under fault conditions, this circuit is tested with a multi-meter and the voltages observed on the test points are given below. Identify the faulty component/s giving fault type, with reasons. [08 marks]

Case	input	TP1	TP2	TP3	TP4
A	0.00	12.00	0.00	0.00	12.00
B	0.00	7.96	0.23	0.83	12.00
C	4.00	8.52	1.80	2.40	3.33
D	4.00	3.60	3.40	3.60	12.00

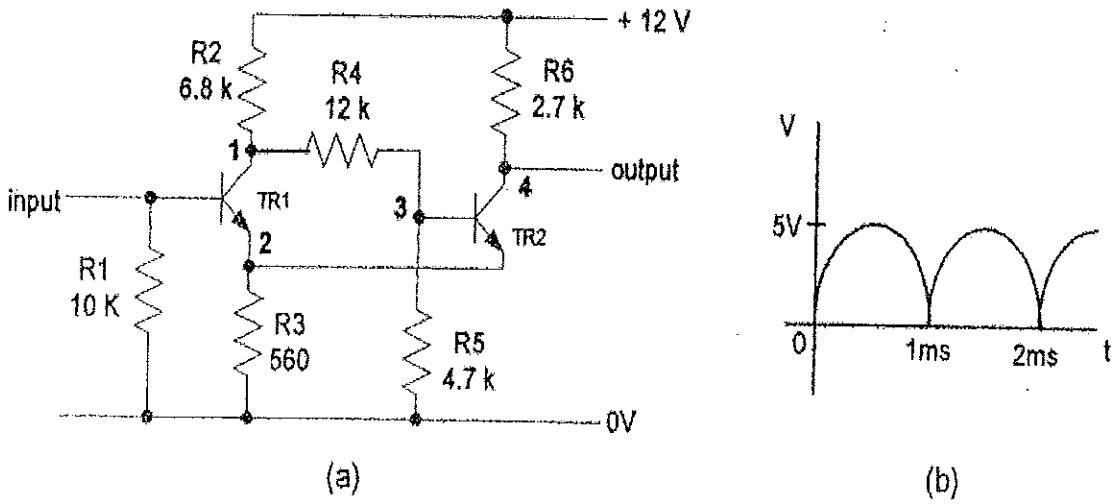

Figure 4

5. Consider the DC voltage regulator circuit shown in Figure 5.

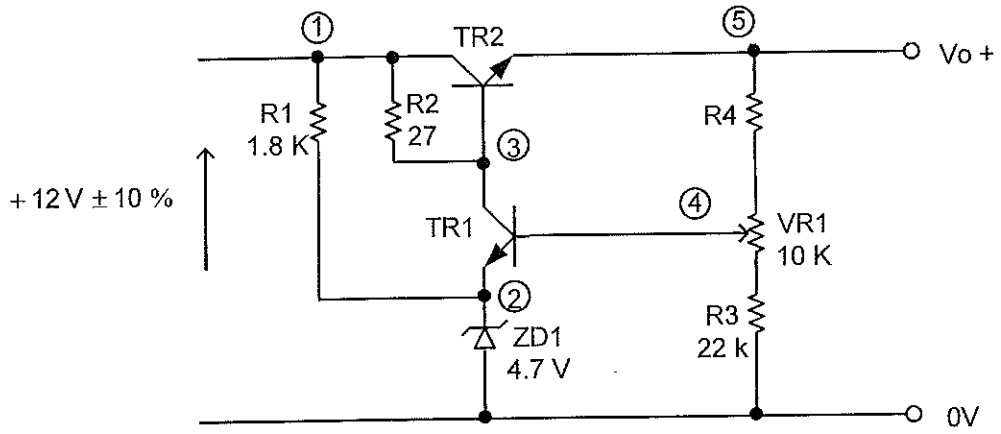

Figure 5

Assume that the current gain of Tr2 and V_{CE} (min) is 30 and 1V respectively. The transistor Tr1 is of high gain type.

(i) Find a suitable value for R4 to obtain maximum guaranteed output voltage and calculate it for this value of R4. [04 Marks]

(ii) Find the minimum output voltage. [01 Mark]

(iii) Calculate the guaranteed maximum load current. [02 Marks]

(iv) Calculate the maximum power dissipation in Tr2, R2 and ZD1. [03 Marks]

(v) Show the implementation of an active current limit circuit for this power supply and find the component values for the worst case of a maximum load current. [02 Marks]

(vi) Following table shows the test point voltages under fault conditions. Determine the faulty component/s with fault type giving reasons. Assume VR1 is set for the maximum output voltage. [08 Marks]

Case	1	2	3	4	5	Output
A	12.00	4.700	11.82	6.140	11.22	No regulation
B	12.00	4.700	10.28	5.300	9.680	Max. load current = 0.9A
C	12.00	4.700	5.900	5.300	5.300	No regulation
D	12.00	4.700	12.00	0	0	No output

6. Consider the circuit shown in figure 6.

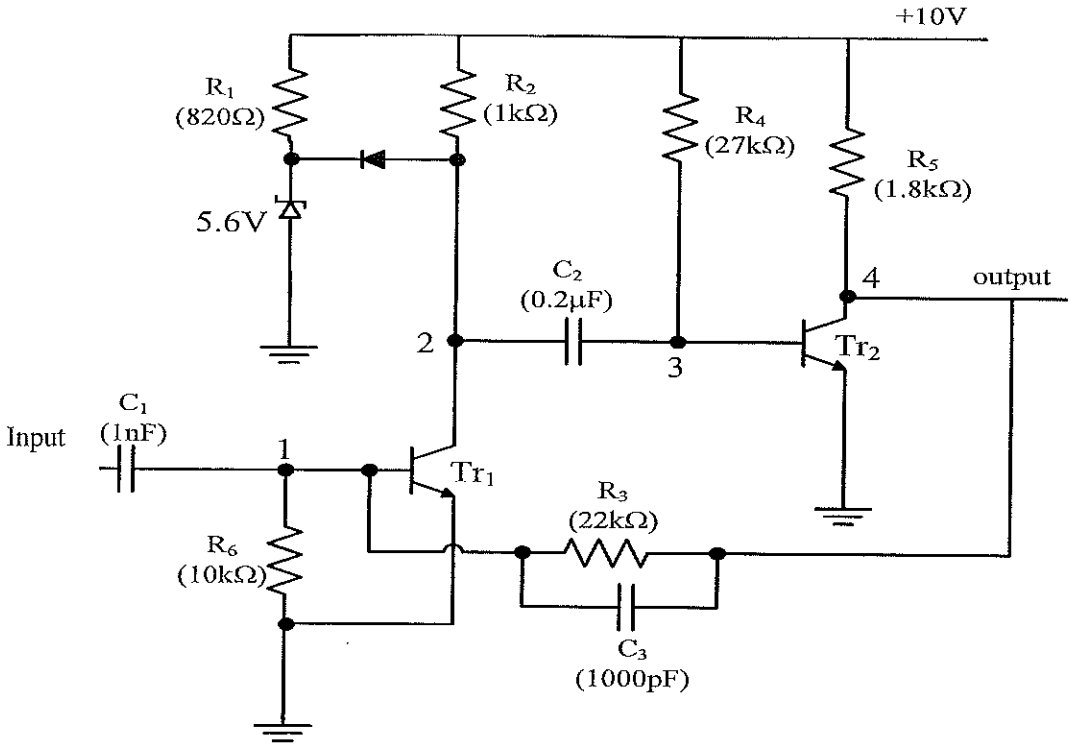

Figure 6

A narrow width pulse train of 250 Hz frequency and +2V height is applied to the input.

a. Draw the waveforms at each test point to a common scale with the input. [04 Marks]
b. Calculate the parameters of the output waveform. [04 Marks]
c. Calculate the voltages at test points, when no signal is applied. [04 Marks]
d. The output is not available under the following fault conditions. State which component is faulty with fault type giving reasons. [08 Marks]

Case	TP1	TP2	TP3	TP4
P	0.2	6.2	0.7	0.2
Q	0.6	0.2	0.7	10
R	0.2	0.6	0.7	0.2
S	0.2	0	0.7	0.2

7. Consider the amplifier, shown in figure 7. The transistors Q1, Q2 and Q3 are of high gain type, while the current gain of Q4 is 50.

a. Calculate Ix and the test point voltages at no signal. **Do not assume** any voltage for a test point. [08 Marks]

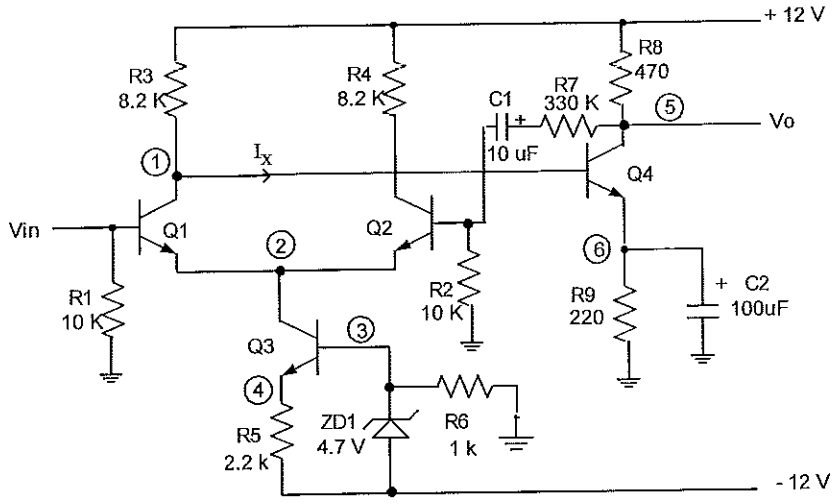

Figure 7

b. A sine wave signal of 1 kHz with 145mV amplitude is applied to the input. Sketch the output signal with the input to a common time scale. Mark the time and voltage values, where necessary. [04 Marks]

c. Following table shows the test point voltages under faulty conditions. Identify the faulty component/s with fault type, giving reasons. [08 Marks]

Case	1	2	3	4	5	6
A	4.56	0	-7.30	-12.0	4.00	3.96
B	0.50	-0.60	-7.30	-7.90	12.0	0
C	0.70	-0.60	-7.30	-7.90	12.0	0.10
D	0.70	-0.60	-7.30	-7.90	0	0.10

8. (a) State the use and limitations of a logic probe. [02 Marks]

(b) Consider the digital circuit shown in figure 8.

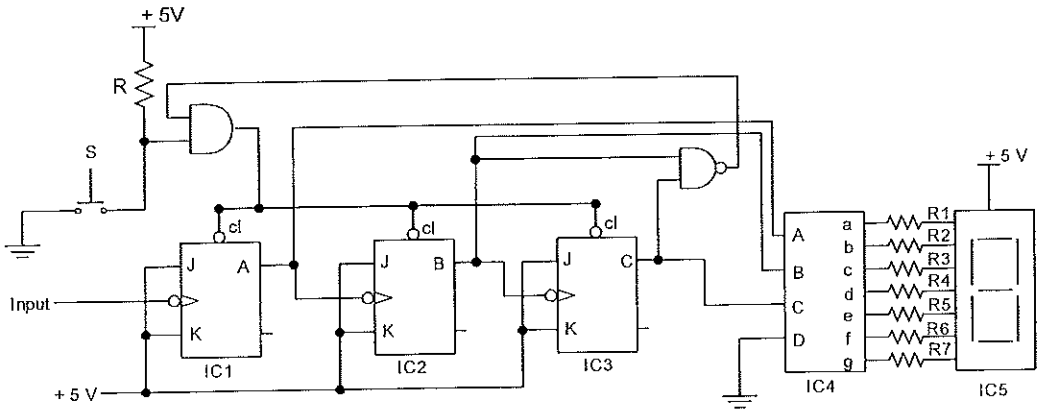

Figure 8

(i) Show the operation of the components IC1, IC4 and IC5, with the aid of tables, using inputs and outputs. [04 Marks]

(ii) After 'S' is pressed, positive pulses of 5V are given to the input. Tabulate the binary states of A, B, C, D and the output of IC5 with each clock pulse. [02 Marks]

(iii) State the faulty component/s for the following fault cases, giving fault type with reasons. [06 Marks]

Case	output of IC5
A	2, 3, 2, 3, 2, 3, ...
B	4, 5, 4, 5, 4, 5, ...
C	0, 1, 2, 3, 4, 5, 6, 7, 0, 1, 2, ...

(iv) In a fault case, a logic probe blinks at A, B and C while the output of IC5 is always '3'. State how the logic probe can be used further to determine the exact faulty component. [04 Marks]

(v) If the resistor R is open, explain the operation of the circuit. [02 Marks]

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