The Open University of Sri Lanka
B.Sc./B.Ed Degree Programme Level-05
Final Examination – 2021/2022
PHU5318 – Electronics for Biology Students
Duration : Two (2) hours

Date: 20 October 2022 **Time: 9.30 p.m.- 11.30 p.m**

Answer Four(4) questions only

(1)

(i) Draw the circuit diagram for a low-pass and high-pass filters. Briefly explain the behaviour of each circuit considering the impedance of the components used **[3 marks x 2]**

(ii) Sketch the following graphs and indicate an important turning point on each graph

(a) Current vs reverse biased voltage for a rectifier diode and

(b) Voltage across a 6.3 V Zener diode vs reversed biased input voltage where a suitable resistor is serially connected with the Zener diode. **[3 marks x 2]**

(iii) Sketch a voltage- time graph for

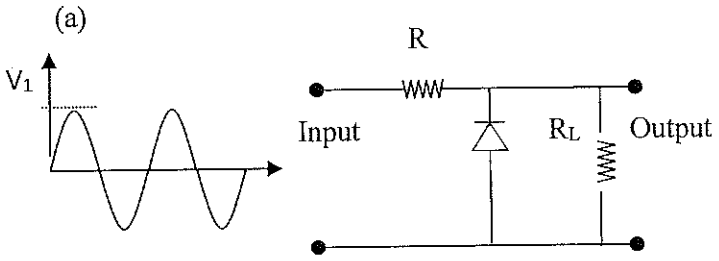
(c) a charging capacitor when it is connected to a 9 V dc voltage source and

(d) then it is discharging. **[2 marks x 2]**

(iv) Sketch voltage-time graphs for half- wave and full- wave rectification. **[2 marks x 2]**

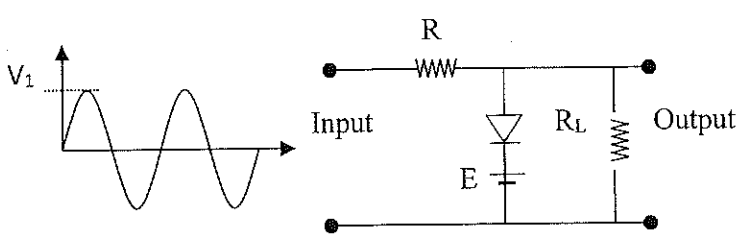
(v) Sketch the output voltage pattens for the following circuits

(a)



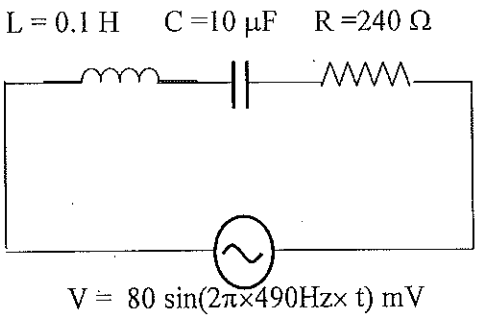
[2 marks]

(b)



[3 marks]

(2) The phase of voltages across an inductor, a capacitor and resistor is different even when the current is same. In the following circuit an inductor , a capacitor and a resistor are serially connected to an alternative voltage source given by $V = 80 \sin(2\pi \times 490\text{Hz} \times t)$ mV .



(i) What is the angular frequency of the voltage source? **[3 marks]**

(ii) Find the total impedance of the circuit. **[4 marks]**

(iii) Using the peak voltage of the voltage source and total impedance ,find the peak current of the circuit. Find the total impedance of the circuit. **[2 marks]**

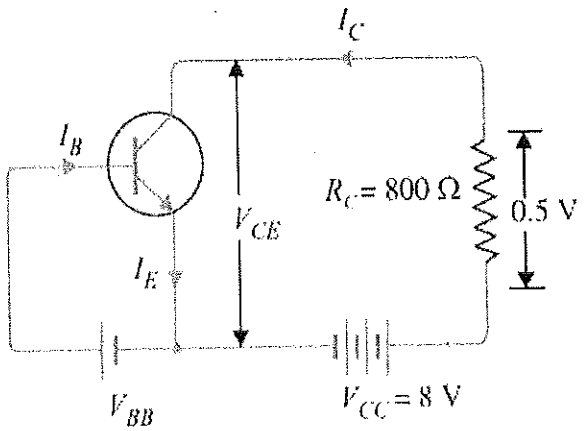
(iv) What are the peak voltages across each component of the circuit. Find the total impedance of the circuit ? **[2 marks x 3]**

(v) Sketch the voltage variation across each component of the circuit on the same voltage – time graph clearly indicating their peak values and phase differences . Find the total impedance of the circuit. **[2 marks x 3]**

(vi) Now the frequency of the connected voltage source is continuously changed . At which frequency , the circuit conducts maximum current in the circuit ? Find the total impedance of the circuit. **[4 marks]**

(3) (i) Briefly explain the material structure of n-type and p-type semiconductors **[4 marks x 2]**

(ii) A npn transistor is connected in common emitter (CE) configuration as shown in the following figure. The circuit is activated with 8 V and the voltage drop across the resistor ; R_C is 0.5 V. The value of $R_C = 800\ \Omega$. The current gain (β) of the transistor is 24 .

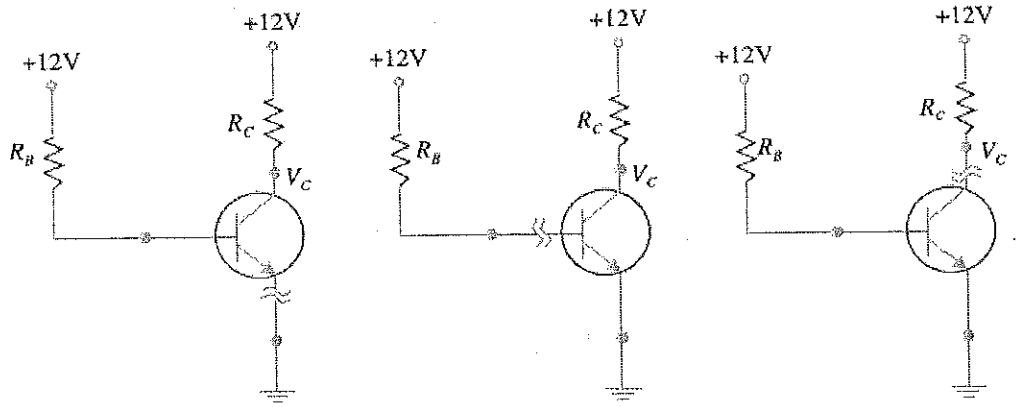


Calculate the followings,

(a) Collector-emitter voltage (V_{CE}) and **[3 marks]**

(b) Base current (I_B) . **[4 marks]**

(iii)The following figures show the open circuit failures in a transistor. The circuit behaviour of the first situation (example) is given.

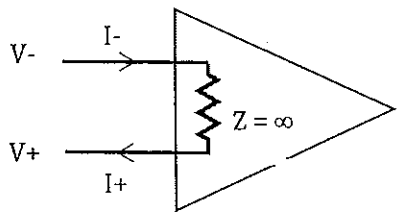


Example :

- Open emitter failure in the transistor.
- Since the base-emitter diode is not forward biased,
- Then ,there can be neither base current nor collector current
  Therefore, there will be no voltage drops across the resistors.
- The voltages at the base, emitter and at the collector leads of the transistor will be 12V.

Write the similar explanation for the other two situations ; (a) and (b). **[5 marks x 2]**

(4) (i)(a) The ideal input impedance (Z) of an operational amplifier is infinitely high (∞).

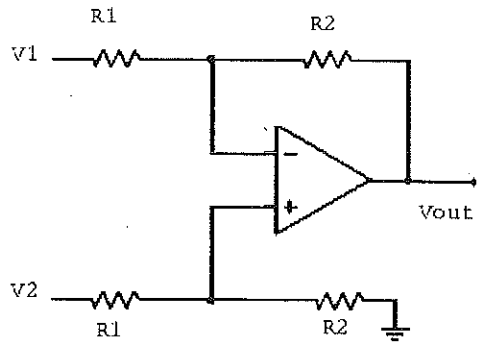


Then write down the conditions for V+ , V- , I+ and I- . **[3 marks x 2]**

(b) Sketch the graph for the output voltage of this operational amplifier for the voltage difference at the input ($V_+ - V_-$). **[3 marks]**

(ii) The following figure shows a diagram of differential amplifier circuit. Write down an expression for the output voltage with the input voltages and resistors.

[4 marks]



(a) If the voltage connected to V2 is 150 mV higher than the voltage at V1 , what is the output voltage when R1 = 10 k and R2 = 100 k ? **[4 marks]**

(b) Derive the expression for the output voltage for inverting amplifier circuit starting from the expression in question (ii)(a). **[4 marks]**

(c) The input impedance of differential amplifier circuit is low and it takes more current from the source which is connected as the input. Extend the given differential amplifier circuit to prevent this problem. **[4 marks]**

(5) In a combinational logic circuit, the state of the output can be defined by the combination of the input states.

(i) Obtain the Boolean expression with AND and OR gates corresponding to the following truth table . **[5 marks]**

Input A	Input B	Output C
0	0	1
0	1	1
1	0	0
1	1	1

(ii) Show that the above expression can be simplified as $C = \bar{A} + A.B$ **[5 marks]**

(iii) Draw the combinational logic circuit for the final expression. **[7 marks]**

(iv) In an automated washing machine, the spinning is automatically operated when the output(O) of the operating unit is at logically 1(one) at with the following conditions are satisfied.

[Condition -1: Water draining is completed (WD = 1) **AND**

Condition -2: water level inside the basing is below the minimum level (L = 0)] **OR**

[Condition-3: Spinning button is pressed (S = 1)]

Write down the truth table for all the possible combinations of WD ,L , S as the inputs and O as the output . **[8 marks]**

(6) J-K flip-flop is a sequential logic device which has two inputs (J and K) with a falling edged clock input (clk) , two controlling inputs (R and S) and two outputs .

(i) What is the difference between combinational and sequential logic circuits? **[3 marks]**

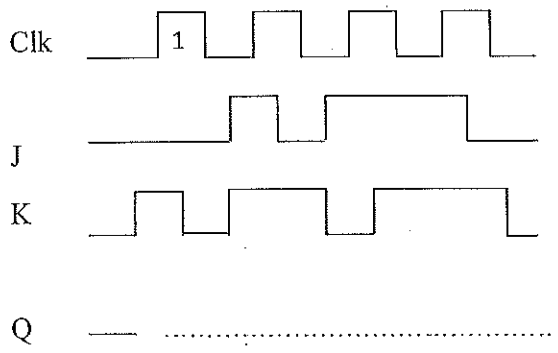
(ii) Name those inputs and outputs in a diagram of a J-K flip-flop. **[4 marks]**

(iii) Write down two advantages of the clock input? **[4 marks]**

(iv) The truth table of a J-K flip flop is given below.

J	K	Output (Q)
0	0	No Change
0	1	0
1	0	1
1	1	Alternate

The above J-K flip flop which consists of a falling edged clock is activated with the following clock (Clk) input pattern where the first Clk pulse is at the left side of the Clk pulse train. Complete the timing diagram for the output (Q) where the initial output is zero.



[5 marks]

(v) Draw the circuit diagram for a three bit up-counter using three falling edge clocked J-K flip flops. **[5 marks]**

(vi) Modify the above counter to reset the output after counting up to five(5) clock pulses.

[4 marks]

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