00146

The Open University of Sri Lanka
Faculty of Engineering Technology
Department of Electrical & Computer Engineering

Study Programme	: Bachelor of Technology Honours in Engineering
Name of the Examination	: Final Examination
Course Code and Title	**: EEX3351 Electronics I**
Academic Year	: 2021/2022
Date	: 27th February 2023
Time	: 0930-1230hrs
Duration	: **3 hours**

General Instructions

1. Read all instructions carefully before answering the questions.
2. This question paper consists of **Five (5)** questions in **Five (5)** pages.
3. Answer **All** the questions.
4. Answer for each question should commence from a new page.
5. Clearly state all your assumptions.
6. This is a Closed Book Test **(CBT).**
7. Answers should be in clear handwriting.
8. Do not use red colour pens.

Q1. Consider the DC power supply circuit in Figure Q1.

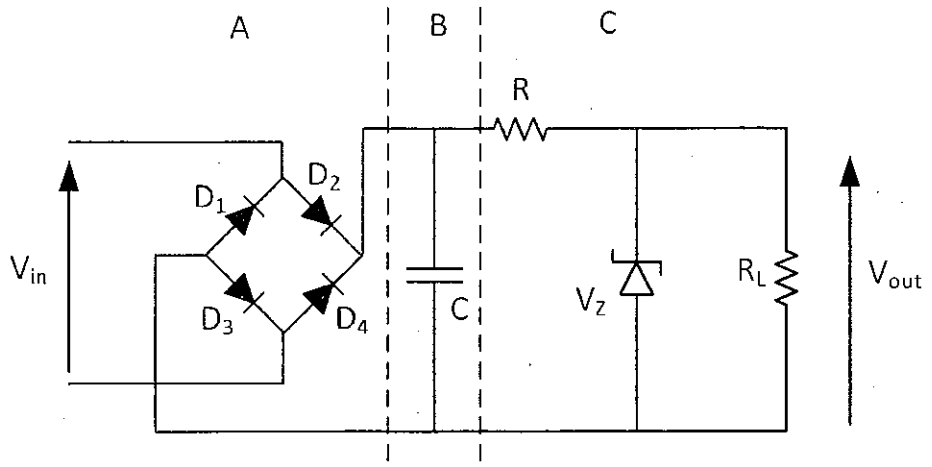


Figure Q1

Let $D_1 \sim D_4$ are identical Si diodes with a forward voltage drop of $0.7V$ in each. $R = 1k\Omega$, $R_L = 10k\Omega$, $C = 10\mu F$. Zenner diode breakdown voltage $V_Z = 5.1V$. V_{in} is a sinusoidal voltage with a peak amplitude of 9V.

(a) Identify the three distinct sub-circuits A, B and C. **(3 Marks)**

(b) Assuming that minimum output value of the section B is 6.1V, draw the output waveforms at the outputs of each A, B and C. **(6 Marks)**

(c) Calculate the minimum and maximum currents flowing through the Zenner diode. **(8 Marks)**

(d) Hence calculate the required maximum power rating for the Zenner diode. **(3 Marks)**

Q2. The single stage BJT transistor amplifier circuit shown in Figure Q2 consists of a Si transistor T having $V_{be} = 0.7V$ and a current gain, $\beta = 100$.

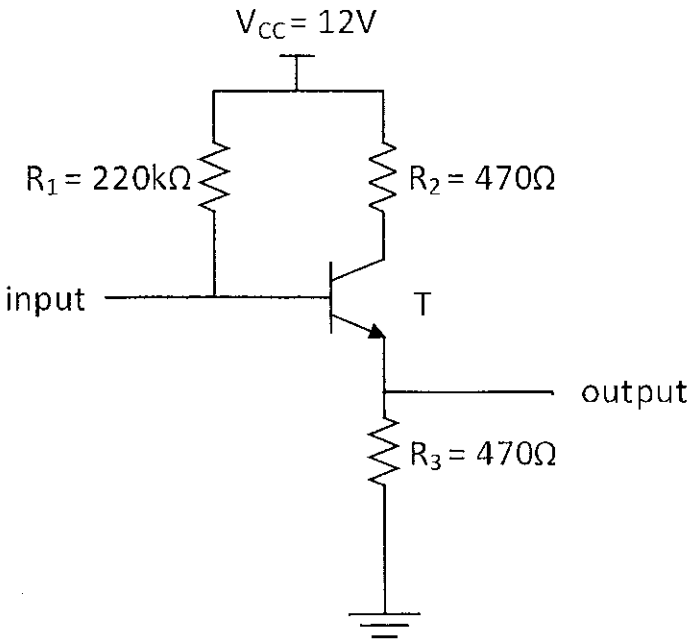


Figure Q2

(a) Write the bias configuration of the circuit shown in Figure Q2. **(2 Marks)**
(b) Calculate the base, collector and emitter currents of the transistor. **(6 Marks)**
(c) Hence calculate the V_{CE} voltage. **(4 Marks)**
(d) Draw the DC load line for the circuit. **(6 Marks)**
(e) Hence, comment on the stability of the amplifier in Figure Q2. **(2 Marks)**

Q3. A small signal circuit is shown in Figure Q3. Let the transistor T1 has $h_{fe} = 50, h_{ie} = 2k\Omega$.

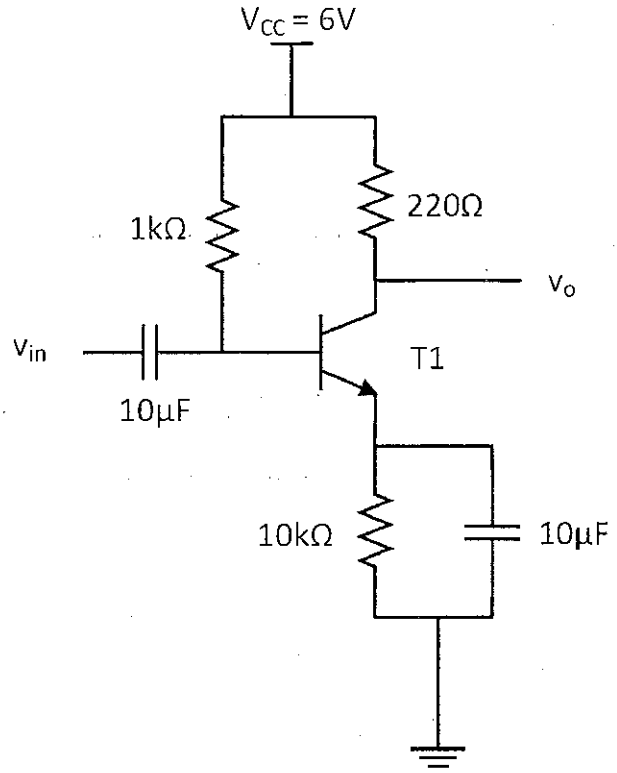


Figure Q3

(a) Draw the AC h parameter equivalent circuit for the amplifier in Figure-Q3. **(5 Marks)**

(b) Using above parameter values, find the following.
i. Current gain **(3 marks)**
ii. Voltage gain **(3 marks)**
iii. Power gain **(3 marks)**
iv. Input impedance **(3 marks)**
v. Output impedance **(3 marks)**

Q4.

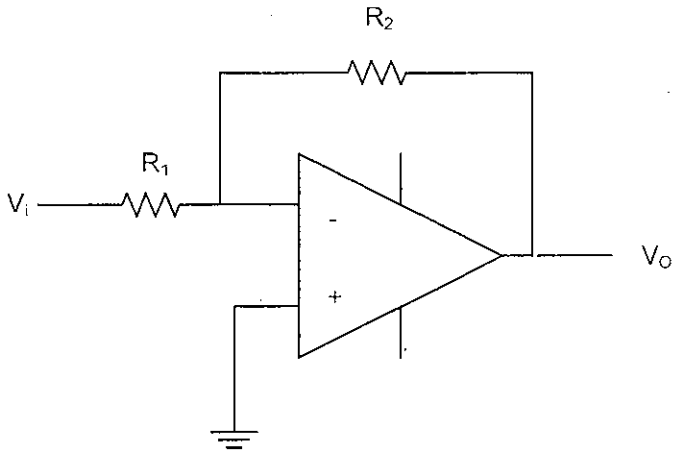


Figure Q4 (a)

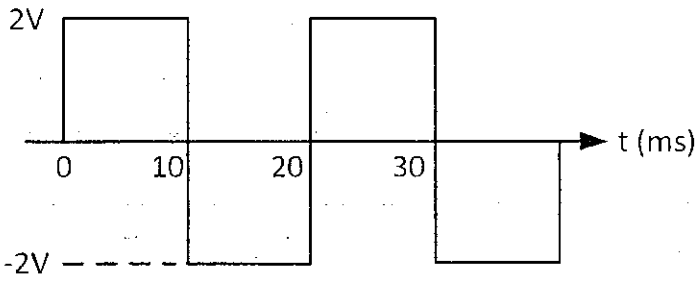


Figure Q4 (b)

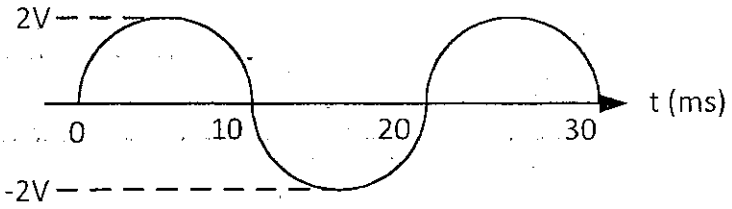


Figure Q4 (c)

(a) List four properties of an ideal operational amplifier. **(4 Marks)**

(b) Derive an expression for the $\frac{V_o}{V_i}$ in the ideal operational amplifier based circuit in Figure Q4 (a). **(6 Marks)**

(c) Let $R_1 = 2.2k\Omega$ and $R_2 = 4.7k\Omega$. Draw the output waveforms with respect to the input signals given in Figures Q4 (b) and Q4 (c). **(2x5 Marks)**

Q5.

(a) Perform the calculation 12-15 in 8 bit 2's complement arithmetic. **(4 Marks)**

(b) Using De Morgan's theorem prove following identities.

i. $AB + \bar{B}C = \overline{(\bar{A} + \bar{B})(B + \bar{C})}$ **(3 Marks)**

ii. $(\bar{A} + \bar{C})(B + \bar{C})[A + B(\bar{B} + \bar{C})] = \overline{AC + \bar{B}C + \bar{A}(\bar{B} + BC)}.$ **(4 Marks)**

(c) Construct Karnaugh maps for the expression $F = ABC + \bar{A}BC + AB\bar{C}$ and find

i. minimum SOP and **(4 Marks)**

ii. minimum POS **(5 Marks)**

expressions.