The Open University of Sri Lanka
Faculty of Engineering Technology
Department of Electrical and Computer Engineering

Study Programme	: Bachelor of Technology Honours in Engineering
Name of the Examination	: Final Examination
Course Codes and Title	**: EEX4351 ELECTRONICS II**
Academic Year	: 2021/22
Date	: 16th February 2023
Time	: 13:30-16:30hrs
Duration	: **3 hours**

General Instructions

1. Read all instructions carefully before answering the questions.
2. This question paper consists of **six (06)** questions in **four (04)** pages.
3. Answer all the questions in Section I (60 marks).
4. Answer only **two (02)** questions in Section II (40 marks).
5. Calculators are permitted to use.
6. This is a Closed Book Test (CBT).
7. Do not use a red colour pen to write the answers.

SECTION I

Question 1 **(30 marks)**

1) Draw the AC equivalent and DC equivalent circuits for the circuit shown in Figure 1. (08 marks)

2) Calculate the values of V_B, V_C, I_E and V_{CE} considering the DC equivalent circuit. Following when the values are given as $R_S = 600\ \Omega$ $R_1 = 47\ \text{k}\Omega$, $R_2 = 10\ \text{k}\Omega$, $R_3 = 300\ \text{k}\Omega$, $R_C = 4.7\ \text{k}\Omega$, $R_E = 100\ \text{k}\Omega$, C_1=10μF , C_2=100μF , C_3=10μF, V_{BE}= 0.7V and β_F= 80. (08 marks)

3) For the circuit shown in Figure 1, suppose the V_B=0V and V_E= 0V readings are shown when measured. Discuss what type of fault is there in this circuit. (10 marks)

4) If R_C is open and the voltage measured at the collector is indicated as 400mV. Explain this observation. (04 marks)

Question 2 **(30 marks)**

1) Derive an expression for the overall voltage gain of a cascaded amplifier with 'k' number stages, where each stage has the same voltage gain A_V and calculate the overall gain value when k=5. (04 marks)

2) If a two stage CE amplifier is designed using two single stage amplifiers, each of which is shown as in Figure 1, Two stages are cascaded with capacitive coupling using $C_c = 1\mu F$. Draw the circuit diagram for the cascaded structure and state any assumptions you make in your answer. (06 marks)

3) Draw the state diagram of a Mealy type design of a binary sequence detector to detect the overlapping sequence of 1011. (08 marks)

4) Design a three bit binary up-down counter using T flip-flops. (12 marks)

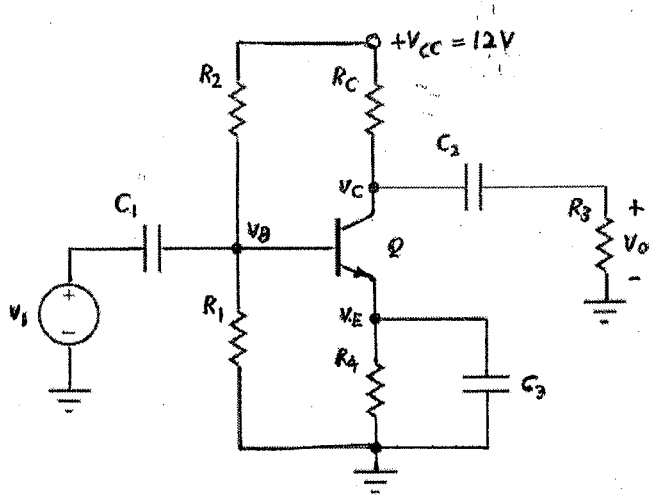


Figure 1: Single Stage BJT amplifier for Question 1

SECTION II

Question 3 **(20 marks)**

1) Describe the V-I characteristic of a typical TRIAC along with its standard symbol to identify the terminals and describe the conduction controlling using a simple circuit. Clearly draw the load voltage variation and the operation of the circuit. (08 marks)

2) Design a binary coded decimal (BCD) to seven segment display decoder unit using standard logic gates. (12 marks)

Question 4 **(20 marks)**

1) Draw the circuit diagram of an OpAmp integrator circuit and derive an expression for the output voltage considering it is an ideal OpAmp. (04 marks)

2) Consider the OpAmp circuit in Figure 2 and derive an expression for the output voltage in terms of the input voltages and the passive elements. Based on your derivation, state the type of behaviour of this circuit. (10 marks)

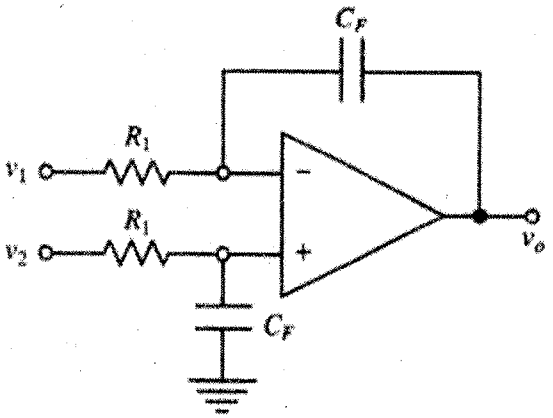


Figure 2: Circuit diagram for Question 4

3) Draw state transition diagram and excitation table of a binary counter which can count the decimal numbers in the order 1, 3, 5, 7, and back to 1. Compute the excitation table using T flip flops. (06 marks)

Question 5 **(20 marks)**

1) Draw the output waveforms for the following input waveforms are fed into the circuit shown in Figure 3. Inputs are sine wave, rectangular pulse, and triangular wave. State the behaviour of the circuit shown in Figure 3. (05 marks)

2) You are asked to build a compact low pass filter to operate at Hz range. Discuss your choice between an active or passive filter design. Provide at least two reasons. (05 marks)

3) Derive an expression for oscillation frequency of a Wein bridge oscillator considering the bridge is balanced. Draw the relevant OpAmp circuit diagram and identify the notations clearly. (10 marks)

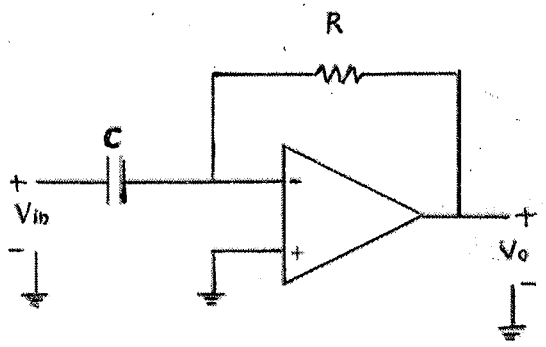


Figure 3: Circuit diagram for Question 5

Question 6 **(20 marks)**

(i) Design a RC-phase shift oscillator that will oscillate at 200Hz. Calculate the values of the feedback resistor and the resistors of the RC sections when 0.5μF capacitor and inverting terminal resistor is given as 20kΩ. Draw the complete circuit diagram with the relevant values of the components. (06 marks)

(ii) Draw the Mealy-type state diagram of a non-overlapping binary sequence detector to detect the sequence 110101. (06 marks)

(iii) Describe the operation of a successive approximation analog to digital converter (ADC) where input ranges from 0V to 12V. In your answer, clearly draw the block diagram of the ADC. (08 marks)