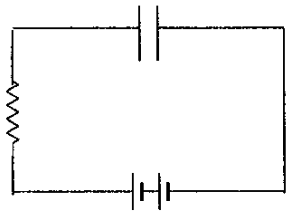
The Open University of Sri Lanka
B.Sc. Degree Programme -Level 05- 2024/2025
Final Examination
Electronics for Biology Students- PHU5318
Duration : Two (2) hours

0099

Date : 02nd December 2024 **Time: 9.30 a.m to 11.30 a.m.**

Answer four (4) questions

(1). A resistor (R) and a capacitor (C) are connected with a DC power supply (V_o) as shown in the following figure.



(i). Write the equation that describes the voltage across the capacitor; $V_c(t)$ as a function of time; t ,when the circuit is in the charging phase.

(ii). If resistance, R = 100 kΩ and a capacitance, C =100 μF with a DC power supply, V_o=10 V, calculate the time constant, $\tau = RC$ of the circuit. What is the simplified unit of τ?

(iii). If the resistance is doubled, then calculate the time constant.

(iv). Calculate the voltage across the capacitor; $V_c(t)$ for these two situations at t = 5 s.

(v). Comparing the above values, sketch the charging curves ;$V_c(t)$ vs t for the above two situations.

(vi). Calculate the current through the circuit at t = 5 s where R = 100 kΩ .

(2). A circuit consisted of an inductor, L = 50 mH and a resistor, R = 10 Ω which are connected in series is connected to an AC power supply with a sinusoidal voltage; $V(t) = V_0 sin(\omega t)$; where V_0 is the peak voltage and ω is the angular frequency.

(i).Calculate the total impedance; Z of the series LR circuit, if ω = 340 rad s^{-1}.

(ii).Calculate the current amplitude I_o in the circuit, given that the peak voltage of the AC source is V_0 = 200 mV.

(iii).Draw a phasor diagram to indicate the phase of voltages across the resistor (V_R) , inductor (V_L) and total impedance (V_Z). Indicate the phase of the current of the circuit in the same diagram.

(iv).Calculate the phase difference between the current and voltage across the total impedance (LR).

(v). If the frequency of the voltage source increases gradually from zero, sketch a graph to show the impedance of each component.

(vi). If a 80 μF capacitor is connected parallel to the inductor, sketch a graph to show the variation of the current through the circuit with the frequency. Write down the value of any specific frequency of your graph.

(3). A non-inverting amplifier circuit is configured with a resistor; R_1 between the input signal (V_{in}) and the non-inverting input of the op-amp, and a feedback resistor; R_2 between the output V_{out} and the inverting input of the op-amp. The op-amp is powered by a dual power supply with +15 V and −15 V.

(i). What are the two golden rules for closed loop operational amplifier circuits.

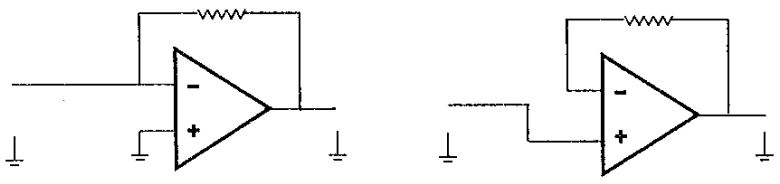
(ii). Draw the circuit diagram of the above non-inverting amplifier including all the given information.

(iii). Derive the expression for the voltage gain; A_v of the non-inverting amplifier in terms of the resistors R_1 and R_2.

(iv). If the input voltage is $V_{in} = 2$ V, $R_1 = 10$ kΩ, and $R_2 = 30$ kΩ, calculate the output voltage V_{out} of the amplifier.

(v). Sketch a graph showing the gain and the resistance ; R_1s while keeping R_2 constant. Show the gains when $R_1 = R_2$ and R_1 goes to infinity.

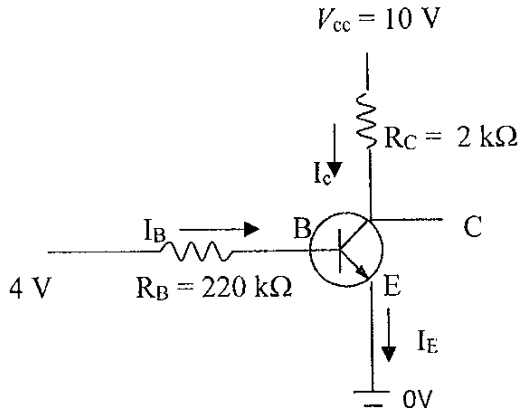
(vi). Give two main different features of each of the following circuits.



(4) (A). (i). Draw atomic structures of *p*-type and *n*-type semiconductors made with Si.

(ii). Draw diagrams showing the *p*-type and *n*-type semiconductor layers in a *NPN* and *PNP* transistors.

(B). Consider the following common-emitter transistor amplifier circuit constructed with an *NPN* transistor where base-emitter voltage; $V_{BE} \approx 0.7$ V

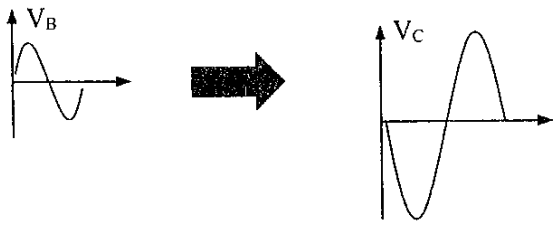


(i). Calculate the Base current; I_B .

(ii). Then calculate the collector current; I_C if current gain; β=1000.

(iii). What is the voltage at C with respect to the ground.

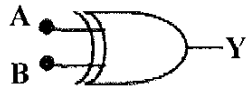
(iv). Briefly explain how the input voltage is inverted at the output; C as shown bellow?



(5) (i). Write down the two Boolean expressions of the De Morgen theorem.

(ii). Considering all the possible combinations of two inputs, verify one of them .

(iii). The symbol and the truth table of Ex-OR gate are given bellow.



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

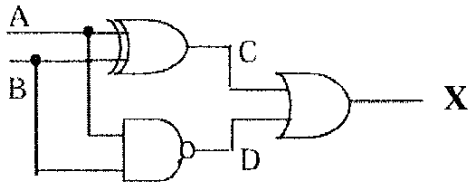
(c)

Using the truth table ,

(a). Obtain a Boolean expression for Y with AND, OR & NOT operations on A and B.

(b). Accordingly construct a combinational logic circuit to produce same output as an Ex-OR gate.

(iv). Obtain the Boolean expression for the output of the following circuit with AND, OR & NOT gates .

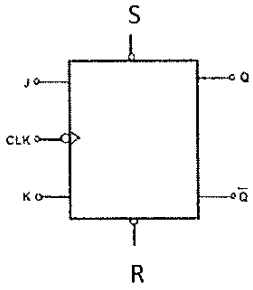


(v) Draw a combinational logic circuit for "full adder ", and justify it by taking two one bit binary numbers; 1 and 1

(6) (i) What is the difference between a positive-edged-triggered and a negative-edged-triggered J-K Flip-Flops?

(ii) This figure shows the symbol of a negative-edged-triggered J-K flip-flop.

Give the truth table for possible J and K input states.



(iii). The above flip-flop is active for its J and K inputs when S and R inputs are at 5 V (state 1). How do you change the output (Q) state to 0 suddenly without CLK ?

(iv). Negative edged flip-flops are used to construct up counters.

Connect 4 flip-flops to construct a 4-bit up counter , showing the required voltages to each pin of all flip-flops.

(v). Draw a timing diagram for the output; Q of the 2^{nd} flip-flop (2^1 binary value) for 12 CLK pulses.

(vi). Modify the diagram given in question(iv) to reset all the outputs to zero after 13 CLK pulses.