The Open University of Sri Lanka
Faculty of Engineering Technology
Department of Electrical & Computer Engineering

097

Study Programme	: Bachelor of Science Honours in Engineering
Name of the Examination	: Final Examination
Course Code	**: EEX4351**
Title	**: Electronics II**
Academic Year	: 2023/24
Date	: 20th March 2025
Time	: 0930-1230hrs

General Instructions

1. Read all instructions carefully before answering the questions.
2. This question paper consists of **Four (4)** questions in **Four (4)** pages.
3. Answer **ALL Questions.**
4. The answer to each question should commence from a new page.
5. Clearly state all your assumptions.
6. This is a Closed Book Test (CBT).
7. Answers should be in clear handwriting.
8. Do not use Red colour pens.

Question 1 **(25marks)**

1. Design a 3-bit synchronous up counter using J-K flip-flops that count in the sequence 0, 1, 3, 5, 6, 7, 0, ...
   i. Determine the number of flip-flops required. *(1 Marks)*
   ii. Draw the state diagram for the counter sequence. *(2 Marks)*
   iii. Create the excitation table showing the present state, next state, and required J-K inputs for each flip-flop. *(3 Marks)*
   iv. Use Karnaugh maps to derive simplified Boolean expressions for each J and K input. *(6 Marks)*
   v. Draw the logic circuit diagram for the counter, including the J-K flip-flops and any additional logic gates required. *(4 Marks)*

2. Consider the design of a digital to analog signal converter for a data acquisition system. The input voltage signal from sensor is in the range of 0-5V. ADC resolution is 12bits and sampling rate is 1000 samples per second. Output analog voltage signal range of 0-10V and DAC resolution is 10bits.

   i. Give two reasons to justify Successive Approximation Register (SAR) ADC method is suitable for this application. *(2 Marks)*
   ii. Calculate the quantization step size of the ADC. *(2 Marks)*
   iii. Select appropriate DAC architecture for the output stage. Explain the two advantages of your chosen architecture. *(3 Marks)*
   iv. Calculate the full-scale output voltage step size for the DAC. *(2 Marks)*

Question 2 **(25marks)**

1. A test circuit for a thyristor is shown in Figure 1. The thyristor parameters are as follows.

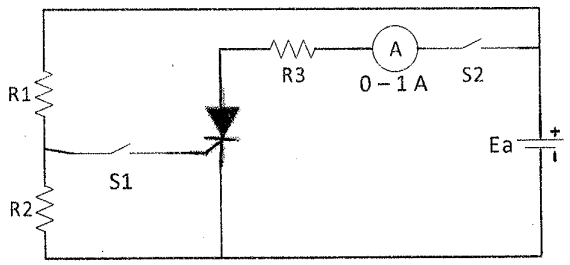


Figure 1

Maximum forward blocking voltage – 100V
Maximum forward current – 2A
Maximum reverse breakdown voltage – 100V
Minimum holding voltage – 2A
Minimum holding current – 25mA
Minimum gate pulse voltage – 3V
Minimum gate pulse current – 10mA
Maximum gate voltage – 8V
Maximum gate current – 100mA

   i. Find suitable values for $Ea, R1, R2$ *and* $R3$. *(11Marks)*
   ii. Explain how to test the thyristor using this circuit. *(4 Marks)*

2. A switch-mode power supply (SMPS) is designed to convert 230V AC mains input to a 12V DC output with a maximum load current of 2A. The SMPS uses a full-wave bridge rectifier followed by a Buck converter operating at a switching frequency of 100 kHz.

   i. Explain two advantages of using an SMPS over a linear power supply for this application. *(2 marks)*
   ii. Draw a block diagram of the SMPS, clearly labeling each stage. *(3 marks)*
   iii. Calculate the peak voltage at the output of the rectifier stage. Assume ideal diodes and negligible transform losses. *(2 marks)*
   iv. Determine the duty cycle required for the Buck converter to produce the desired 12V DC output. *(3 marks)*

Question 3 **(30marks)**

1.A two-stage amplifier circuit is shown in Figure 2. Assume that two transistors are identical. Source impedance is Rs.

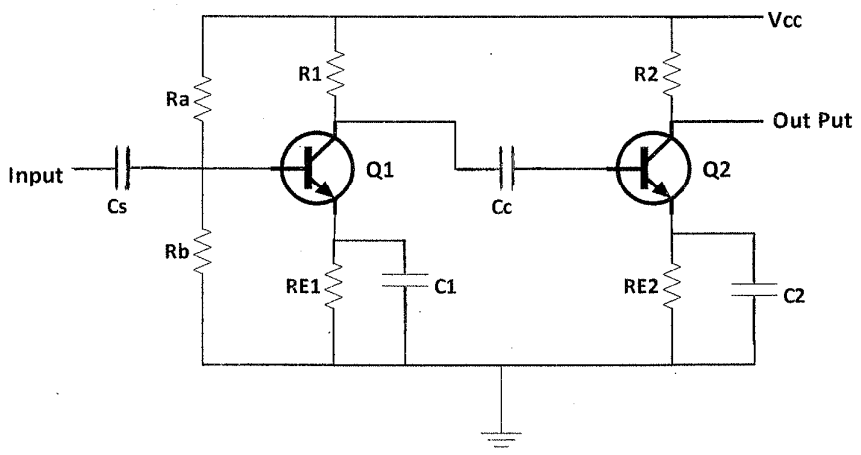


Figure 2

   i. Draw a high frequency equivalent circuit for above circuit using π-parameter model. *(5 Marks)*
   ii. Obtain an expression for the voltage gain at high frequencies using Miller's theorem. *(15Marks)*
   iii. The π-parameter of the transistors are given below.
   $R_{bb'} = 100\Omega$, $R_{b'e} = 1k$, $C_{b'e} = 100pF$, $C_{b'c} = 3pF$, $G_m = 50mA/V$
   If R1 =R2 =2k and Rs = 50 Ω, Find the upper 3dB point of the Amplifier.
   Stage clearly any approximations that you make. *(5 Marks)*

2. Calculate the maximum output power for a Class B push-pull amplifier with a supply voltage of ±15V and a load resistance of 8Ω. *(3 Marks)*

3. Small Signal transistor amplifier is shown in Figure 3.

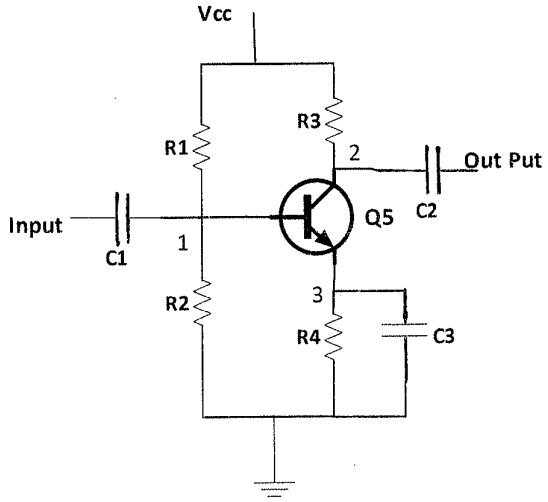


Figure 3

In a faulty condition it was observed Test Point (TP) voltages as follows.

TP	1	2	3
Measured Reading (V)	0.7	0.14	0

Giving reasons, identify the faulty component/s. *(2 Marks)*

Question 4 (20 marks)

1.

i) State two advantages of active filters against passive filters. *(2 Marks)*

ii) Derive voltage transfer function of the circuit shown in Figure 4. Assume R1=R2, Find the relationship between C1 and C2 for this circuit to act as Butterworth filter. Obtain an expression for the cut-off frequency. *(15Marks)*

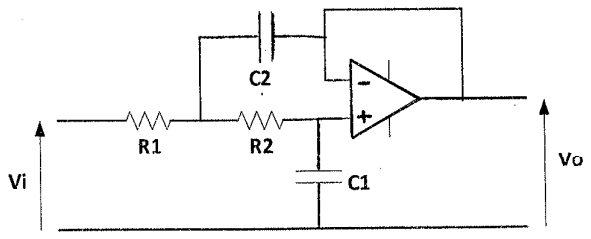


Figure 4

The second order Butterworth filter transfer function for the normalized gain is given by

$$1/\left[\left(s/\omega_0\right)^2 + \sqrt{2}\left(s/\omega_0\right) + 1\right]$$

Where, $S = j\omega$

2. State three conditions that must be satisfied for sustain oscillations in a Wien bridge oscillator. *(3 Marks)*