

The Open University of Sri Lanka
Faculty of Engineering Technology
Department of Electrical and Computer Engineering



Study Programme : Bachelor of Science Honours in Engineering
Name of the Examination : Final Examination
Course Code and Title : **EEX5536 Computer Architecture**
Academic Year : 2023/24
Date : 16th March 2025
Time : 09:30 – 12:30 hrs.
Duration : **3 hours**

General Instructions

- Read all the instructions carefully before answering the questions.
- This question paper consists of **five (5)** questions in **four (4)** pages.
- Answer all the questions.
- All questions carry equal marks.
- Answer for each question should commence from a new page.
- Answers should be in clear handwriting and do not use Red colour pen.
- Clearly state your assumptions, if any.
- This is a **Closed Book Test (CBT)**.
- For calculation-based questions, show all intermediate calculation steps clearly leading to your final answer.

Q1

- (a) Explain the concept of instruction pipelining and its significance in processor performance, with the help of a diagram illustrating the process.

[05 Marks]

- (b) Briefly explain the different types of delays that can occur in a pipeline.

[05 Marks]

- (c) What is the difference between superscalar architecture and pipelining?

[02 Marks]

- (d) Assuming that A nonpipelined processor has a clock rate of 2.5 GHz and an average CPI (cycles per instruction) of 4. An upgrade to the processor introduces a five-stage pipeline. However, due to internal pipeline delays, such as latch delay, the clock rate of the new processor has to be reduced to 2 GHz.

- I. What is the speedup achieved for a typical program?
- II. What is the MIPS rate for each processor?

[08 Marks]

Q2

- (a) Given a program with both serial and parallelizable sections, briefly explain, in point form, how factors like the fraction of parallelizable code and the number of cores in a multi-core processor system impact the program's overall performance and speedup.

[05 Marks]

- (b) Discuss, in point form, how factors such as cache architecture and memory bandwidth influence the overall speedup in a multi-core processor system.

[03 Marks]

- (c) A benchmark program is executed on a 3 GHz processor, completing a total of 14 million instructions. The program consists of four main types of instructions. Based on a program trace experiment, details on each instruction type, including its CPI and its percentage in the Instruction Mix (IM), are given below.

Instruction Type	Instruction Mix	CPI	IM
Arithmetic and logic		1	60%
Load/store with cache hit		2	18%
Branch		4	12%
Memory reference with cache miss		8	10%

Now, consider running the program as eight parallel tasks or threads, each executing approximately the same number of instructions. The execution takes place on an 8-core system, where each core has the same performance as the originally used single processor. Due to coordination and synchronization, an additional 250,000 instructions are executed in each task. The instruction mix remains the same as in the original example, but the CPI for memory reference instructions with cache misses increases to 12 cycles due to memory contention.

- I. Calculate the average Cycles Per Instruction (CPI) for the given program.
- II. Determine the corresponding Million Instructions Per Second (MIPS) rate.
- III. Compute the speedup factor achieved with parallel execution.
- IV. Compare the actual speedup factor with the theoretical speedup predicted by Amdahl's Law, explaining any differences.

[12 Marks]

Q3

- (a) Compare the pros and cons of direct-mapped and set-associative cache memory organizations in CPU architecture, using a table.

[06 Marks]

- (b) Briefly explain the concept of cache coherence and its importance in multi-core or multi-processor systems.

[04 Marks]

- (c) Assume The average memory access time for a microprocessor with a single-level cache is 2.4 clock cycles. If data is present and valid in the cache, it can be found in 1 clock cycle. If data is not found in the cache, 80 clock cycles are needed to fetch it from off-chip memory.

Design engineers are aiming to improve the average memory access time by 65% and are considering adding a second level of cache on-chip. The second level of cache would take 6 clock cycles to access, and its addition does not affect the first-level cache's access patterns or hit times. Off-chip memory accesses would still require 80 additional clock cycles.

- I. Calculate the current average memory access time for the microprocessor with the given single-level cache configuration.
- II. Calculate the new average memory access time if the second-level cache is added and the target improvement in average memory access time (65%) is achieved.
- III. Discuss the impact of adding a second-level cache on performance, considering the given parameters. How does the two-level cache affect the overall memory access time?

[10 Marks]

Q4

- (a) Compare the advantages, disadvantages, and typical usage of the four main I/O methods in computer systems.

[12 Marks]

- (b) Consider a processor with programmed I/O that executes instructions at a rate of 0.7 MIPS. An I/O subroutine for writing to a USB disk requires 50000 instructions and the disk has a total latency of 125 microseconds. A disk request is initiated every second of task time. What is the efficiency of this system?

[04 Marks]

- (c) In systems that include DMA (Direct Memory Access) modules, DMA access to the main memory is often given higher priority than CPU access to the main memory. Is this statement correct? Justify your answer

[04 Marks]

Q5

- (a) Briefly Explain the key characteristics of the memory hierarchy in a computer system and discuss the importance of having a memory hierarchy in terms of performance and efficiency.

[04 marks]

- (b) What are the key factors that influence the performance of a memory system? Discuss their impact in point form, focusing on cache organization, memory bandwidth, and access latency?

[03 marks]

- (c) Consider a magnetic disk drive with 8 surfaces, 250000 tracks per surface, and 500 sectors per track. Sector size is 512 bytes. The average seek time is 6.5ms, the track-to-track access time is 4.7ms, and the drive rotates at 7200 rpm. Successive tracks in a cylinder can be read without head movement.

- i. What is the disk capacity?

[02 marks]

- ii. What is the data transfer rate?

[03 marks]

- iii. What is the average access time? Assume this file is stored in successive sectors and tracks of successive cylinders, starting at sector 0, track 0 of cylinder i.

[04 marks]

- iv. Estimate the time required to transfer a 5-MB file.

[04 marks]

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