

The Open University of Sri Lanka
Faculty of Engineering Technology
Department of Electrical and Computer Engineering



Study Programme : Bachelor of Science Honours in Engineering
Name of the Examination : Final Examination
Course Code and Title : EEX7434 Digital Signal Processing
Academic Year/Semester : 2023/2024
Date : 15th March 2025
Time : 1330-1630h
Duration : 3 hours

General instructions

1. This is a closed book examination.
 2. There are four (04) compulsory questions in this question paper. Answer all the questions.
 3. Do not use red colour pen to write the answers.
 4. Please remember to write your registration number in the space provided above and in the answer script. **Do not write your name.**
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Question 1**[20 marks]**

A discrete-time system is described by the difference equation: $y(n) - 0.5y(n-1) = x(n)$ where $x(n)$ is the input and $y(n)$ is the output.

1. Evaluate the system's transfer function $H(z)$ using the Z-transform. [05 marks]
2. Determine the impulse response $h(n)$ of the system. [05 marks]
3. Analyze the stability of the system using the pole locations. [05 marks]
4. Evaluate the system's output if the input is $x(n) = 2^n u(n)$. [05 marks]

Question 2**[30 marks]**

1. Explain the Gibbs phenomenon in digital filter designing. [05 marks]
2. State the possible solutions to overcome the effects of Gibbs phenomenon. [05 marks]
3. Design a 6th-order FIR filter using the Hamming window with sampling frequency of 5kHz and cutoff frequency of 1.2 kHz. Show the numerical calculations of ideal impulse response and the filter coefficients. [20 marks]

Question 3**[30 marks]**

Answer the following questions related to digital signal processors (DSP) architectures and functionalities.

1. List four features of a DSP that differentiates it from a general-purpose microprocessor. [03 marks]
2. Compare the three (03) common architecture types of DSPs based on access to data and instructions. [05 marks]
3. Describe the role of the Multiply-Accumulate (MAC) unit in DSPs. [02 marks]
4. State the reason why DSPs use circular buffering. [02 marks]
5. State the five (05) main stages of an execution cycle in DSP. [05 marks]
6. Describe pipelining in DSP. [03 marks]
7. Draw the block diagram of a general programmable DSP architecture with direct memory access. [10 marks]

Question 4**[20 marks]**

Consider a discrete-time sequence: $x(n) = \{1, 2, 3, 4\}$ where $x(n)$ is defined for $n = 0, 1, 2, 3$.

1. Compute the 4-point Discrete Fourier Transform (DFT) $X(k)$. [05 marks]
2. Verify the result by computing the Inverse Discrete Fourier Transform (IDFT). [05 marks]
3. Interpret the frequency-domain representation of $X(k)$. [10 marks]