

The Open University of Sri Lanka
Faculty of Engineering Technology
Department of Electrical and Computer Engineering



Study Programme	: Bachelor of Technology Honours in Engineering/ Bachelor of Science Honours in Engineering
Name of the Examination	: Final Examination
Course Code and Title	: EEX3336 – Communications and Computer Technology
Academic Year	: 2022/23
Date	: 09 th February 2024
Time	: 0930-1230hrs
Duration	: 3 hours

General Instructions

1. Read all instructions carefully before answering the questions.
 2. This question paper contains four (4) questions on five (5) pages.
 3. Answer ALL questions.
 4. The answer to each question should commence from a new page.
 5. This is a Closed Book Test (CBT).
 6. Answers should be in clear handwriting.
 7. Do not use Red colour pen, and clearly state your assumptions, if any
-

Answer ALL questions.

1)

- a) Describe Von Neuman and Harvard computer architectures by giving diagrams.
(06 marks)
- b) Explain how arithmetic and logic operations are handled in a microprocessor using appropriate instructions from Annexure. You must show a complete cycle of an instruction execution. You may use the standard abbreviations of the special purpose registers.
(12 marks)
- c) Figure 1 shows the Body Weighing Scale in the market. According to its specifications, the maximum capacity is 180kg, and the graduation rate is 100g. So, it indicates the weights with one decimal place.

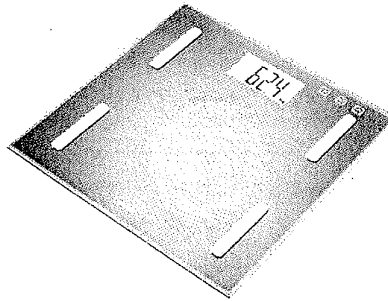


Figure 1. Body Weighing Scale

- (i) Determine the number of bits required to store weight values with one decimal place.
- (ii) If the design has limited the storage capacity to 10-bit registers, what is the maximum error of the weights in grams?
- (iii) To introduce a value-added feature to this scale, it is proposed to show the average body weight of a week. However, it takes only four days of the week to make the calculations simple. Accordingly, how many bits does it need for registers involved in the calculation? Maintain the same error as in the question 1.c.ii).
- (iv) Using the instructions in the Annexure, write an assembly program segment to calculate the average body weight of the week. Assume body weights are stored in four consecutive memory locations.

(22 marks)

2) Write all relevant intermediate steps when answering questions from (a) to (d)

- a) Convert the following decimal integer and fraction to binary.

(i) 57

(01 mark)

(ii) 0.225 (Truncate answer at 4th bit after binary point)

(02 marks)

- b) Perform the following binary arithmetic operations.

- (i) $1010100 + 1000111$ (show the carry bits clearly) (02 marks)
- (ii) $11101 * 1001$ (show the partial products clearly) (04 marks)

c)

- (i) Calculate the decimal equivalent of the negative number -101011.01_2 (01 mark)
- (ii) Represent the number obtained above 2.c.i), in IEEE754 binary floating point single precision format. Show the steps clearly. (03 marks)

d) Perform the following using binary 2's complement techniques.

- (i) $28 - 43$ (03 marks)
- (ii) $-4.5 - 6.25$ (04 marks)

3)

a) Briefly explain similarities and differences between TCP/IP model and OSI reference model. (Use suitable diagram for your answer.) (03 marks)

b) Medium Access Control protocols are used to provide fair, shared access to all the attached stations of a network.

- (i) State 2 commonly used Medium Access Control protocols.
- (ii) Explain the working principle of one of the above-mentioned protocols. (05 marks)

c) DTE and DCE are important when it comes to cross over and straight through cables. Explain the meaning of DTE and DCE in network devices and how it influences the choice between cross over and straight through cables for connecting two devices. (02 marks)

d) IP addressing is used in computer networks to distinctly identify the networks and the devices.

- (i) Compare the two addressing schemes, IPv4 and IPv6.
- (ii) Identify the bit allocation for network ID and host ID for different classes in IPv4.
- (iii) What are two types of subnetting used with IPv4 address scheme?
- (iv) For the given IP address $171.123.135.127/20$, find the network address, number of subnets and number of hosts available for each subnet. (10 marks)

4)

a) Modulation and demodulation are very important in communication systems.

- (i) Briefly explain the terms modulation and demodulation.
- (ii) State 2 important needs of modulation.
- (iii) Draw the appropriate basic block diagram of a communication system with modulator and demodulator blocks. (06 marks)

b) State three radio wave propagation modes.

(03 marks)

c) A message Signal $m(t) = 5 \cos 3000\pi t$ modulates carrier frequency to produce a frequency modulated (FM) signal with a frequency deviation ratio (m_p) of 2.

(i) Find the modulating frequency.

(ii) Frequency deviation

(iii) What is the estimate of the bandwidth of the FM Signal, and find the K_f ?

(iv) If the message signal $m(t)$ is replaced with new message signal $m(t) = (12 \cos^2 2000\pi t - 6)$, what is the estimate of the bandwidth of new FM signal?

(08 marks)

d) If the input power of the system given below is 1mW and the overall net gain is 20dB, find the output power in mW and attenuation loss X marked in Figure 2.

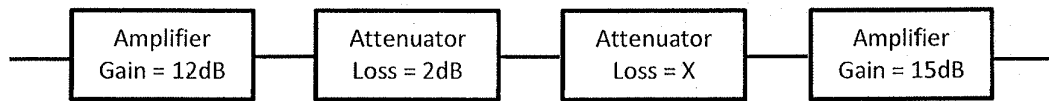


Figure 2.

(03 marks)

ISA of Accumulator Architecture

Mnemonic	Syntax	Operation	Description	Add Mode	Flags affected
Arithmetic instructions					
ADD	ADD AM x	Addition	$Acc \leftarrow Acc + op$	#, default	ZF, OF, SF, PF = 1
SUB	SUB AM x	Subtraction	$Acc \leftarrow Acc - op$	#, default	ZF, OF, SF, CF, PF = 1
MUL	MUL AM x	Signed multiplication	$Acc(16\text{ bit}) \leftarrow Acc(8\text{ LSBs}) * op(8\text{ LSBs})$	#, default	ZF, SF, PF = 1, OF, CF = 0
DIV	DIV AM x	Unsigned division	$Acc \leftarrow Acc / op2$	#, default	ZF, SF, PF = 1, OF, CF = 0
INC	INC	Increment by 1	$Acc \leftarrow Acc + 1$	#, default	OF, SF, ZF, PF = 1
Logical instructions					
AND	AND AM x	Bit-wise And	$Acc \leftarrow Acc \text{ AND } op$	#, default	OF, CF = 0; SF, ZF, PF = 1
OR	OR AM x	Bit-wise OR	$Acc \leftarrow Acc \text{ OR } op$	#, default	OF, CF = 0; SF, ZF, PF = 1
XOR	XOR AM x	Bit-wise XOR	$Acc \leftarrow Acc \text{ XOR } op$	#, default	OF, CF = 0; SF, ZF, PF = 1
SHL	SHL	Shift left by 1-bit	$CF \leftarrow Acc(\text{MSB}), op \leftarrow Acc(14\text{ down to }0) \& 0$	Implied (A)	CF = bit shifted by Acc. SF, ZF, PF = 1.
SHR	SHR	Shift right by 1-bit	$CF \leftarrow Acc(\text{LSB}), Acc \leftarrow 0 \& Acc(15\text{ down to }1)$	Implied (A)	CF = bit shifted by Acc. SF, ZF, PF = 1.
ROL	ROL	rotate left by 1-bit	$CF \leftarrow Acc(\text{MSB}), op \leftarrow Acc(14\text{ down to }0) \& CF$	Implied (A)	CF = bit shifted by Acc. SF, ZF, PF = 1.
ROR	ROR	rotate right by 1-bit	$CF \leftarrow Acc(\text{LSB}), Acc \leftarrow CF \& Acc(15\text{ down to }1)$	Implied (A)	CF = bit shifted by Acc. SF, ZF, PF = 1.
NOT	NOT	One's complement negation	$Acc \leftarrow \text{NOT } Acc$	Implied (A)	none
Control Transfer instructions					
Conditional Branches					
JC	JC d	Jump if carry	If CF = 1 then $PC \leftarrow PC + \text{Operand}$	PC relative	none
JOF	JOF d	Jump if over-flow	If OF = 1 then $PC \leftarrow PC + \text{Operand}$	PC relative	none
JS	JS d	Jump if Sign	If SF = 1 then $PC \leftarrow PC + \text{Operand}$	PC relative	none
JP	JP d	Jump if parity	If PF = 1 then $PC \leftarrow PC + \text{Operand}$	PC relative	none
JZ	JZ d	Jump if result is zero	If ZF = 1 then $PC \leftarrow PC + \text{Operand}$	PC relative	none
Unconditional branch					
JUMP	JUMP d	Jump	$PC \leftarrow PC + \text{Operand}$	PC relative	none
Loops					
LOOPZ	LOOPZ d	Loop until zero	Count $\leftarrow$ Count - 1, IF Count = 0; Loop termination ELSE; $PC \leftarrow PC + \text{operand}$	PC relative	none
Calls and Returns					
CALL	CALL d	Procedure call	implied return address $\leftarrow PC$, $PC \leftarrow$ immediate address	*	none
RETURN	RETURN	Return from procedure	$PC \leftarrow$ Contents of implied return address	**	none
Miscellaneous instructions					
NOP	NOP	No operation		none	none
Data Movement instructions					
LOADacc	LOADacc AM x	Copy the operand to the accumulator	Immediate: $Acc \leftarrow op$; Direct: $Acc \leftarrow \text{memory}(op)$	#, default	none
STOREacc	STOREacc AM x	Copies the accumulator to the memory address	Direct: $\text{Memory}(op) \leftarrow Acc$ Indirect: $\text{Memory}[\text{memory}(op)] \leftarrow Acc$	default, &	none

* Immediate operand is used as the jumping location.

** Contents of the implied return address is used as the jumping location

x- Memory Address or immediate value, d- Displacement

Addressing Modes -AM

Immediate

Direct

Indirect

default (blank)
&