The Open University of Sri Lanka
Faculty of Engineering Technology
Department of Electrical and Computer Engineering

Study Programme	:	Bachelor of Science Honours in Engineering
Name of the Examination	:	Final Examination
Course Code and Title	:	**EEX5536 Computer Architecture**
Academic Year	:	2024/25
Date	:	06th March 2026
Time	:	1400-1700h
Duration	:	3 hours

General instructions

1. **Read all instructions** carefully before answering the questions.
2. This question paper consists of **Five (5)** questions in **Four (4)** pages.
3. Answer **all** questions.
4. All questions carry equal marks.
5. Answer for each question should commence from a new page.
6. Answers should be in **clear handwriting** and do not use red colour pen.
7. Clearly state your assumptions, if any.
8. For calculation-based questions, **show all intermediate calculation steps** clearly leading to your final answer.
9. This is a Closed Book Test (CBT).
10. Non-programable calculators are allowed.

Question 01

a. For each major type of pipeline hazard, describe the detection methods and possible solutions. Provide your answer clearly using a table. (12marks)

b. Consider a single-cycle processor. The latencies for the instruction fetch, instruction decode, ALU operation, memory access, and write-back stages are 20 ps, 10 ps, 20 ps, 20 ps, and 10 ps, respectively. (08marks)

I. Assuming a pipelined processor with the same stage delays and no pipeline overheads, calculate the speedup achieved by pipelining compared to the non-pipelined processor. Clearly show your calculations.

II. Suppose the ALU operation time is reduced by 25%. Will this change the speedup obtained from pipelining? If yes, calculate the new speedup. If no, briefly justify your answer.

III. Now assume the ALU operation takes 25% more time than its original latency. Determine whether the speedup changes and, as above, calculate the new speedup or briefly justify your answer, if not.

Question 02

a. Discuss, in point form, how hardware characteristics and software parallelization approaches influence the overall performance of a multi-core processor system. (04 marks)

b. Discuss the validity of Moore's Law in the context of modern computing systems. (02 marks)

c. A new embedded processor runs at a clock frequency of 4 GHz. A standard benchmark program consisting of 50 million instructions is executed on this processor to evaluate its performance. (14 marks)

The instruction set is divided into four classes, and the results from the program trace experiment are provided as follows:

Instruction Class, CPI, Instruction Mix (%) respectively:

- Integer Arithmetic, 1, 45%
- Floating Point, 5, 20%
- Memory Access (Load/Store), 3, 25%
- Branch / Control, 2, 10%

I. Calculate the Average Cycles Per Instruction (CPI) for this benchmark program.

II. Determine the Total Execution Time (in milliseconds) and the MIPS rating for this processor.

III. A compiler optimization is proposed that reduces the number of Floating-Point instructions by 50%. However, this optimization causes the CPI of the remaining Floating-Point instructions to increase from 5 to 6. Calculate the Speedup achieved by this optimization.

IV. Instead of the compiler optimization in part (iii), the hardware team proposes upgrading the Floating-Point Unit (FPU) to make it run 4 times faster. Calculate the fraction of total execution time ($f_{enhanced}$) consumed by Floating Point instructions in the *original* design.

V. Using Amdahl's Law, calculate the overall system speedup achieved by above (part (iv)) hardware upgrade.

Question 03

a. Provide short answers to the following questions. (18 marks)

I. A legacy PCI bus uses a shared, parallel bus architecture. What are the significant disadvantages of this design compared to a modern point-to-point serial bus like PCIe?

II. What are the primary functions of a "turnaround cycle" (or bus idle cycle) in a shared parallel bus protocol?

III. In the context of modern high-speed interconnects (Ex: PCI Express, SATA), describe the key advantages of serial transmission over parallel?

IV. What are the primary roles of the UART (Universal Asynchronous Receiver/Transmitter) in a traditional serial port used for devices like an old mouse or modem?

V. In a bidirectional parallel port (Ex: EPP or ECP mode), what additional hardware features are required compared to a simple output-only port?

VI. Why is the transfer of data from a disk drive's internal buffer to the system's main memory typically performed using Direct Memory Access (DMA)?

b. Discuss the key advantage of placing a network controller directly on the PCI Express (PCIe) bus in a modern system. (02 marks)

Question 04

a. Compare Interrupt-driven I/O and DMA in terms of: CPU involvement, Data transfer efficiency, Hardware complexity and Suitable application scenarios. (04 marks)

b. Consider a processor with programmed I/O that executes instructions at a rate of 0.1 MIPS. An I/O subroutine for writing to a disk requires 10,000 instructions and the disk has a total latency of 100 ms. A disk request is initiated every second of task time. What is the efficiency of this system? (06 marks)

c. Briefly explain the following terms related to cache memory (04 marks)

I. Address Mapping
II. Replacement Policy

d. A hierarchical memory system that uses cache memory has cache access time of 50 nano seconds, main memory access time of 300 nano seconds, 75% of memory requests are for read, hit ratio of 0.8 for read access and the write-through scheme is used. What will be the average access time of the system both for read and write requests? (06 marks)

Assume cache access time is not included in main memory access time.

Question 05

a. Briefly explain why modern computer systems use hierarchical memory organization instead of single-level memory and describe how each level of the memory hierarchy addresses the fundamental design trade-offs in computer systems. (05 marks)

b. Assume a hard disk drive has 3 disks (4 surfaces: the two outer disks only have 1 usable surface each and the inner one has two.) Each surface is divided into 400 tracks and sectors per track is 80. The sector size is 512 bytes. It is spinning at 3600 rpm. (15 marks)

I. How long would it take for a read/write head to read one sector?

II. Assume that it takes on the average 30 msec (milliseconds, 1 msec = .001 sec) to seek to any track. Taking into account the seek time, rotational latency and the time to read one sector, how long would it take this disk drive to fetch and read an arbitrary track?

III. If files are comprised of sectors scattered all over the disk drive, how long would it take to read a file consisting of 1,064,960 bytes?

IV. If files are arranged so that the sectors in a file are as contiguous as possible and it only takes 3 msec to seek to a new track, how long would it take to read the same file of 1,064,960 bytes?

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