The Open University of Sri Lanka
Faculty of Engineering Technology
Department of Electrical and Computer Engineering

Study Programme	:	Bachelor of Science Honours in Engineering
Name of the Examination	:	Final Examination
Course Code and Title	:	**EEX4351 Electronics II**
Academic Year	:	2024/25
Date	:	3rd March 2026
Time	:	0930-1230h
Duration	:	3 hours

General instructions

1. Read all instructions carefully before answering the questions.
2. This question paper consists of **Four (4)** questions in **Four (4)** pages.
3. Answer **all** questions.
4. All questions carry equal marks.
5. Answer for each question should commence from a new page.
6. This is a Closed Book Test (CBT).
7. Use standard notations.
8. Assume components are ideal unless otherwise stated.

Question 1 (25 marks)

Design a Finite State Machine (FSM) for a Battery Charging Controller that controls the Charging Module based on the digital signals provided by the Battery Monitoring Unit. Refer to Figure 1 for the system architecture.

- The charging controller must operate according to the following rules:
  - When the battery percentage falls below 80%, fast charging must be enabled.
  - When the battery percentage reaches 80% or above, slow charging must be activated.
  - When the battery becomes fully charged (100%), charging must be disabled.
- Charging Module consists of two pins

  Enable Pin (EN)
  EN = 1 → Charging enabled
  EN = 0 → Charging disabled

  Mode Select Pin (M)
  M = 1 → Fast charging mode
  M = 0 → Slow charging mode
- Monitoring Unit provides the following digital signals

  B80 → 1 if Battery ≥ 80%, otherwise 0
  B100 → 1 if Battery = 100%, otherwise 0
  B100 = 1 and B80 = 0 when no battery is connected

a. Identify suitable states for the battery charging controller (FSM) and clearly explain the function of each state. (5 marks)
b. Draw a complete state transition diagram including the inputs and outputs. Design the FSM as a Moore machine. (7 marks)
c. Construct the corresponding excitation table including Present State, Input Conditions (B100, B80), Next State, Flip-Flop Inputs, and Output Signals (EN, M). Use D flip-flops for the design. (6 marks)
d. Design and draw the logic circuit for the controller. Simplify the logic expressions for the flip-flop inputs and controller outputs using K-maps. (7 marks)

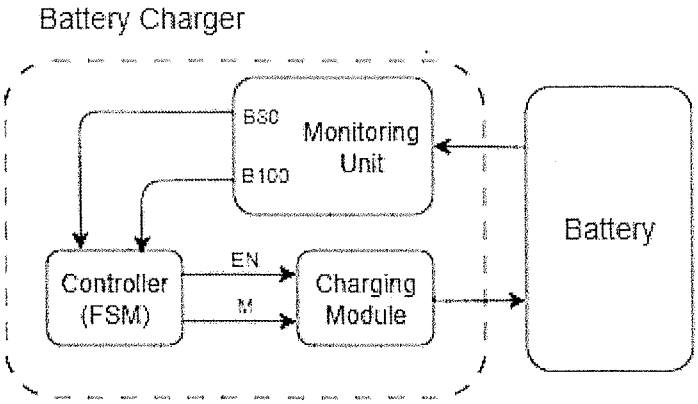


Figure 1: Architecture of the battery charger

Question 2 (25 marks)

A biomedical monitoring system measures variations in electromagnetic field intensity near the human body. However, the measured signal is heavily contaminated by a 60 Hz interference signal generated by nearby 240 V power lines. To suppress this unwanted interference, an active filter is to be designed.

a. Identify a suitable filter topology to remove the 60 Hz interference and briefly justify your answer. (4 marks)

b. Sketch the ideal magnitude response of the filter if the Q factor is 3. (5 marks)

c. Design a second-order high-pass filter and a second-order low-pass filter using the cutoff frequencies identified in part (b), based on the Sallen-Key topology. The required passband gain of each filter is 10dB. Assume ideal op-amps. (10 marks)

d. Draw the complete circuit diagram of the required filter. (6 marks)

Question 3 (25 marks)

A transducer converts a physical quantity into a voltage with a maximum amplitude of 5 mV (peak-to-peak). The output is connected to an ADC with an input range of 0–1 V. The following BJT amplifier is used for signal conditioning.

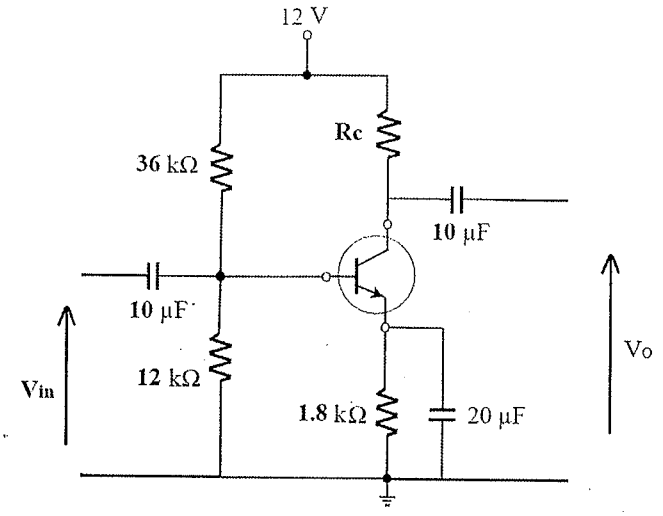


Figure 2: BJT Amplifier

a. Simplify the biasing network using Thevenin's theorem. Given that β = 99, determine the quiescent collector current I_{CQ} and transconductance g_m.
(6 marks)

b. Draw the high-frequency small-signal equivalent circuit using the Hybrid-π model. Given:
$r_o = 100\ k\Omega$
$C_{be} = 40\ pF$
$C_{bc} = 1.5\ pF$
Assume $r_{bb'} \approx 0$, $r_{b'c} \approx \infty$. (5 marks)

c. Derive the expression for midband voltage gain. Hence, determine the required value of R_C. (7 marks)

d. Determine the maximum operating frequency of the amplifier. Justify your answer using calculations. (7 marks)

Question 4 (25 marks)

1) The circuit shown in Figure 3 uses a Silicon Controlled Rectifier (SCR) to control a DC load. The SCR has the following specifications.

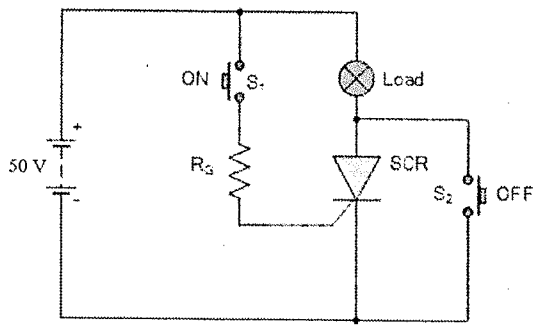


Figure 3: Power controlling circuit

Minimum gate trigger current, $I_{GT(min)} = 20$ mA
Minimum gate trigger voltage, $V_{GT(min)} = 3$ V
Maximum forward blocking voltage = 100 V
Maximum reverse breakdown voltage = 100 V
Maximum forward current, $I_{F(max)} = 2$ A
Minimum holding voltage = 2 V
Minimum holding current = 25 mA

a. Design a suitable gate resistor R_G so that the SCR is reliably triggered. Calculate both the required resistance value and the minimum power rating of the resistor. (5 marks)
b. Determine the minimum value of load resistance that can be connected safely without damaging the SCR. (4 marks)
c. Briefly explain how switch S_2 operates to turn OFF the SCR. (3 marks)

2. A DC power supply of 5 V is used to power an electronic system through a DC–DC converter. The converter operates in continuous conduction mode (CCM) at a switching frequency of 50 kHz. The system requires a regulated output voltage of 12 V and a maximum load current of 2 A.

a. Which DC-DC converter topology is most suitable for this purpose? Draw the circuit and explain your answer. (4 marks)
b. Derive the voltage equation for the converter and calculate the duty cycle value required. (5 marks)
c. If the peak-to-peak inductor current ripple is limited to 30% of the average inductor current, calculate the required inductance value. (4 marks)

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