The Open University of Sri Lanka
Faculty of Engineering Technology
Department of Electrical and Computer Engineering

0178

Study Programme	:	Bachelor of Science Honours in Engineering
Name of the Examination	:	Final Examination
Course Code and Title	:	**EEX3336 Communications and Computer Technology**
Academic Year	:	2024/25
Date	:	17th February 2026
Time	:	0930-1230h
Duration	:	3 hours

General instructions

1. Read all instructions carefully before answering the questions.
2. This question paper consists of **Four (4)** questions in **Five (5)** pages.
3. Answer **all** questions.
4. The first question is allocated 40 marks, and the other three questions are allocated 20 marks each
5. Answer for each question should commence from a new page.
6. This is a Closed Book Test (CBT).
7. Non-programmable calculators are allowed.

Question 01

a. I. Briefly explain the Fetch-Execute Cycle of the Accumulator based CPU. (09 marks)

II. With reference to the fetch–execute cycle, explain how instruction execution proceeds in each of the following addressing modes: Immediate, direct, Indirect with help of diagrams.

b. Briefly explain the key enhancements and characteristics of fourth-generation computers (starting in the 1970s), with reference to: Hardware technology, Software development and impact on users & applications. (06 marks)

c. Consider a robotic arm joint angle monitoring system. (25 marks)

The system uses a high-resolution rotary encoder that measures the angular position of a joint. The encoder's output covers a range of –90° to +90° relative to the neutral position. The encoder outputs the angle as a digital value.

I. If the encoder outputs a 14-bit unsigned digital value, what is the smallest angular change (in degrees) that the encoder can detect? Assume all 14 bits are used efficiently, meaning the highest possible integer value uses all bits without unused leading bits.
[04 marks]

II. The system stores the last 12 angular position readings in a circular buffer. Each buffer location holds one angle reading. How many bits are required to store the buffer index?

Tip: The buffer index is stored separately and indicates the next location to write in the buffer.
[03 marks]

III. To detect sudden jerks (rapid movements), the system compares the current angle with the previous angle. If the absolute difference exceeds 8°, a *JERK_WARNING* is triggered. Given the range of −90° to +90°, how many bits are required to store the signed difference between two angle readings?
[04 marks]

IV. Draw a **single flowchart** showing the algorithm for the assembly program segment that does the following:

- If a jerk warning is triggered (from part III), store JERK_FLAG = 1 in memory location 0x5A; otherwise store 0.
- Assume the current angle and previous angle are available in memory.

[08 marks]

V. Write an assembly program for the algorithm in part (d). Use the **Accumulator-based Instruction Set Architecture (ISA)** provided in **Appendix A.**
[06 marks]

Question 02

a. Do the following calculations. Show the intermediate calculation steps. (06 marks)

I. Convert 10001.0001_2 to its decimal equivalent.
II. Convert 545.79_{10} to its binary equivalent.
III. Convert 1010011.0111_2 to its Hexadecimal equivalent.

b. Perform the following operations. Show all intermediate steps clearly. (06 marks)

I. Perform binary multiplication of the following: 100.101 × 110

II. Perform binary division of the following: 101.01 ÷ 110

III. Find the 'x' of the following equation by using the 2's complement method.

x = 32 − 51

c. Convert -726.357 numbers to IEEE 754 Single precision format. Show the intermediate calculation steps clearly. (05 marks)

d. Explain why special coded representations such as Binary-Coded Decimal (BCD) and ASCII were introduced in computing systems, despite the existence of simpler binary representations. (03 marks)

Question 03

A medium-sized organization plans to upgrade its network infrastructure to support web-based applications, internal file sharing, and secure communication between multiple departments located in the same building.
The organization has been assigned the IP address block 172.16.40.0/22 and requires separate network segments for the following departments:

Administration – 180 hosts
Engineering – 90 hosts
Finance – 40 hosts
IT Support – 20 hosts

a. Define a computer network and state TWO advantages of implementing a structured network in an organization. (3 marks)

b. When an employee accesses a secure web application hosted on an internal server, explain how data travels through the OSI reference model, from the client application to the server. (4 marks)

c. Perform subnetting on the given IP address block to meet the departmental requirements. (10 marks)
For each department, clearly specify:

I. Network address
II. Subnet mask
III. First usable host address
IV. Last usable host address
V. Broadcast address

State any assumptions made during subnet allocation.

d. The above organization plans to use switches, routers, and wireless access points in its network. Briefly explain the function of EACH device and justify where it would be used within this organization's network. (3 marks)

Question 04

a. Define analog modulation and classify the main types of analog modulation. (2 marks)

b. With the aid of mathematical equations, explain how the modulation index is defined for (4 marks)

I. Amplitude Modulation (AM) and
II. Frequency Modulation (FM).

Clearly identify all symbols used in the equations.

c. An amplitude-modulated signal is applied to a linear envelope detector. The measured envelope voltages are:

$$V_{max} = 14\,V \;\; V_{min} = 6\,V$$

I. Calculate the modulation index of the AM signal. (2 marks)
II. Determine whether the signal is under-modulated, perfectly modulated, or over-modulated, and justify your answer. (2 marks)
III. If the carrier amplitude is kept constant and the modulation index is increased beyond one, explain why the envelope detector output becomes distorted, even though the transmitted power increases. (4 marks)

d. A frequency-modulated signal is given by:

$$v_{FM}(t) = 20sin\,[2\pi(80 \times 10^6)t + \beta sin\,(2\pi \times 4 \times 10^3 t)]$$

The maximum frequency deviation of the carrier is known to be 24 kHz.

I. Calculate the FM modulation index β. (2 marks)
II. Determine the modulating frequency. (2 marks)
III. Estimate the bandwidth of the FM signal. (2 marks)

Appendix A

Accumulator Architecture

Mnemonic	Syntax	Operation	Description	Add Mode	Flags affected
Arithmetic instructions					
ADD	ADD AM x	Addition	Acc ← Acc + op	#,&,default	ZF, OF, SF, PF =1
SUB	SUB AM x	Subtraction	Acc ← Acc - op	#,&,default	ZF, OF, SF, CF, PF =1
MUL	MUL AM x	Signed multiplication	Acc (16 bit) ← Acc(8 LSBs) * op(8 LSBs)	#,&,default	ZF, SF, PF =1. OF, CF=0
DIV	DIV AM x	Unsigned division	Acc ← Acc / op2	#,&,default	ZF, SF, PF =1. OF, CF =0
INC	INC	Increment by 1	Acc ← Acc + 1	#,&,default	OF, SF, ZF, PF=1
Logical instructions					
AND	AND AM x	Bit-wise And	Acc ← Acc AND op	#,&,default	OF, CF=0; SF, ZF, PF =1
OR	OR AM x	Bit-wise OR	Acc ← Acc OR op	#,&,default	OF, CF =0; SF, ZF, PF =1
XOR	XOR AM x	Bit-wise XOR	Acc ← Acc XOR op	#,&,default	OF, CF=0; SF, ZF, PF =1
SHL	SHL	Shift left by 1-bit	CF ← Acc (MSB), op← Acc (14 down to 0) & 0	Implied (A)	CF= bit shifted by Acc. SF, ZF, PF=1.
SHR	SHR	Shift right by 1-bit	CF ← Acc (LSB), Acc ← 0 & Acc (15 down to 1)	Implied (A)	CF= bit shifted by Acc. SF, ZF, PF=1.
ROL	ROL	rotate left by 1-bit	CF ← Acc (MSB), op← Acc (14 down to 0) & CF	Implied (A)	CF= bit shifted by Acc. SF, ZF, PF=1.
ROR	ROR	rotate right by 1-bit	CF ← Acc (LSB), Acc ← CF & Acc (15 down to 1)	Implied (A)	CF= bit shifted by Acc. SF, ZF, PF=1.
NOT	NOT	One's compliment negation	Acc ← NOT Acc	Implied (A)	none
Control Transfer instructions					
Conditional Branches					
JC	JC d	Jump if carry	If CF =1 then PC ← PC + Operand	PC relative	none
JOF	JOF d	Jump if over-flow	If OF =1 then PC ← PC + Operand	PC relative	none
JS	JS d	Jump if Sign	If SF =1 then PC ← PC + Operand	PC relative	none
JP	JP d	Jump if parity	If PF =1 then PC ← PC + Operand	PC relative	none
JZ	JZ d	Jump if result is zero	If ZF =1 then PC ← PC + Operand	PC relative	none
Unconditional branch					
JUMP	JUMP d	Jump	PC ← PC + Operand	PC relative	none
Loops					
LOOZ	LOOZ d	Loop until zero	Count ← Count – 1, IF Count =0; Loop termination ELSE; PC ← PC + operand	PC relative	none
Calls and Returns					
CALL	CALL d	Procedure call	implied return address ← PC, PC ← immediate address	*	none
RETURN	RETURN	Return from procedure	PC ← Contents of implied return address	**	none
Miscellaneous instructions					
NOP	NOP	No operation		none	none
Data Movement instructions					
LOADacc	LOADacc AM d	Copy the operand to the accumulator	Immediate: Acc ← op; Direct: Acc ← memory (op)	#, default	none
STOREacc	STOREacc AM d	Copies the accumulator to the memory address	Direct: Memory (op) ← Acc Indirect: Memory {memory (op)} ← Acc	default, &	none

*Immediate operand is used as the jumping location.
**Contents of the implied return address is used as the jumping location
x- Memory Address or immediate value, d- Displacement

Addressing Modes -AM

Immediate	#
Direct	default (blank)
Indirect	&

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