THE OPEN UNIVERSITY OF SRI LANKA
BACHELOR OF TECHNOLOGY - LEVEL 6
ECX6236 – PROCESSOR DESIGN
FINAL EXAMINATION 2005

DURATION: THREE HOURS

0036

Date : 29th April 2006 **Time : 0930 - 1230 Hrs**

Answer **three** questions including the question in Section A and selecting two from the Section B.

Section A

The question in this section is compulsory (70 marks).

1. You have to design a special graphic processor, which is for constructing display panels with LEDs in a matrix. The processor sends a 32-bit word from the output port along with a pulse from the *Data Ready* pin. The width of the pulse is less than the clock period. The information given from the output port can be used to light 32 LEDs on a display panel. The set of bits to the output port is taken from four adjacent bytes of the internal memory. As soon as the subsequent four adjacent bytes are ready to send, the processor will generate the next pulse at the *Data Ready* pin. This will continue until the last memory location and thereafter it will loop back to the beginning of the memory location to repeat the same. The user can define the beginning and the last memory location of the image (information) at the very beginning of his/ her program.

   When you are designing the processor, you must keep provision to store information (bit pattern of the image) into the internal memory. In addition, user must be able to set delays in between outputs. However there should be an instruction to send a number of 32-bit output words continuously and the user will be able to provide as to how many words to be sent in the instruction itself. This instruction will actually start sending output words from the beginning of the memory location though the instruction does not contain any address of a memory location in it. The processor calculates the address of the memory location automatically for the next output word. User program must be stored in the internal memory of the processor as well.

   The internal memory of the processor may be limited to 1 MB. You may give a simple design of the processor which is capable of doing the functions as described above. When you are answering the questions state all assumptions you made (if any) clearly.

   a) Identify the necessary instructions needed for this processor and design a set of instructions for the processor.
   b) Using your instruction set write a simple program to display an image on a panel having LEDs arranged in 64 columns by 30 rows. Make sure to use all your instructions in the instruction set.
   c) Identify all input and output signals of the processor you are going to design.
   d) Draw a block diagram of the processor. Clearly, give all functions of each block inside the processor. Briefly, describe the function of the processor.
   e) Identify entities, which will be used for writing a VHDL code for the processor.
   f) Write down the behavioural/ structural architecture for each entity.
   g) Estimate the minimum clock frequency of the processor if it is used for a panel 320x200 LEDs in size for real time images. Assume that 25 frames have to be generated for this purpose.

Section B

*Answer **two** questions from this section. Each question carries 15 marks.*

2.

a) What are the advantages of using HDL for VLSI design?
b) Write a Behavioural VHDL code for the *D Flip-flop* of Fig 1.1.

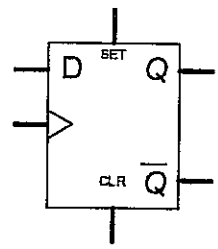


Fig 1.1

c) Write Structural VHDL code for an 8-bit register using D flip-flops given in Fig. 1.1.

3.

a) What are the steps that you follow to design a hardwired control unit of a processor?
b) Construct the state diagram of the control unit of the special processor in Question 1.

4.

a) What are the advantages in each modelling technique, Structural modelling and Behavioural modelling, and give examples?
b) What are the characteristics of a systolic architecture?
c) Show how you can implement a systolic architecture using VHDL giving an example.

5.

a) Describe how you are estimating the cost of a processor. Derive equations where necessary.
b) Compare and contrast SIMD and MIMD Architecture.
c) What are the major advantages of designing systolic architectures when considering the manufacturing of processors?

Annexure

Syntax of selected instructions of the VHDL

```
ARCHITECTURE architecture_name OF entity_name IS
  [declaration part]
BEGIN
  Concurrent statements part
END architecture_name
```

```
CASE expression IS
  WHEN value=> statements;
  WHEN value=> statements;
  WHEN OTHERS statements;
END CASE;
```

```
COMPONENT component_name
  PORT (port1_name : port1_type;
        port2_name : port2_type;
        …);
END COMPONENT [component_name];
```

```
ENTITY entity_name IS
  PORT (port1 : port1_type;
        port2 : port2_type;
        …);
END entity_name;
```

```
IF condition THEN
  Sequence of statements
  {ELSIF condition THEN
     Sequence of statements}
[ELSE
  Sequence of statements]
END IF;
```

```
LIBRARY library_name;
```

```
Instance_label: component_name PORT MAP (first_port, second_port,
                                         third_port, …);
Instance_label: component_name PORT MAP (formal1=> actual1,
                                         formal1=> actual1,
                                         formal1=> actual1, …);
```

```
[process_label:] PROCESS (signal1, signal2, …)
                   [declaration part]
                 BEGIN
                   Sequential statements part
                 END PROCESS;
```

```
SIGNAL signal_name : signal_type;
```

```
TYPE type_name;
```

```
USE library_name.type_expression.inclussion;
```

```
WAIT FOR time_expression;
```

WAIT ON **signal1, signal2, …;**

WAIT UNTIL ***condition;***

```
WHILE condition LOOP
  Sequential statements
END LOOP;
```