THE OPEN UNIVERSITY OF SRI LANKA
BACHELOR OF TECHNOLOGY - LEVEL 05
ECX5236 – COMPUTER ARCHITECTURE
FINAL EXAMINATION 2008

110

DATE: 05th April 2009 **TIME: 0930 – 1230 hours**

Answer any ***five*** questions. All questions carry equal marks.

1. An application running on a 1GHz pipelined processor has 55% load-store, 30% arithmetic, and 15% branch instructions. The individual CPIs of these instructions are 5, 4 and 4, respectively.

(i) Determine the overall CPI of this program execution on the given processor.

(ii) Find the MIPS rating of the processor.

(iii) A new embedded version of the processor is being modified to operate at 600 MHz. In this new version, the individual CPIs of load-store and arithmetic instructions are remaining unchanged. However, the individual CPI of branch instructions is getting stretched to 6 clock cycles. A new compiler is also developed for the new processor which reduces of load-store instructions to 30% and arithmetic instructions to 25% for the given application.

(a) Determine the overall CPI of this program execution on the new processor together with the new compiler technology.

(b) Determine the MIPS rating of the new processor with the new compiler technology.

2.

(i) Explain the *Amdahl's law* which can be used to calculate the performance gain. Your answer must be enriched with the relevant formula.

(ii) Suppose there are $n\,(n \geq 1)$ enhancements for a new architecture. Let t_i and s_i are the fraction of time used and the speedup of the i^{th} enhancement, $(i = 1, 2, \ldots n)$ respectively. Derive the expressions for n enhancements.

(a) The total time that not use for enhance. I.e. Time for Un-enhance.

(b) The total time taken for the enhancement.

(c) Show the overall speedup (S) of the architecture is

$$S = \left[1 - \sum_i t_i + \sum_i \frac{t_i}{s_i}\right]^{-1}$$

(iii) Three enhancements with the following speedups are proposed for a new architecture: Assume that there are independent each other.

	E1	E2	E3
Speedup	30	20	10

(a) If each E1 and E2 uses 30% of the execution time, what fraction of the time must E3 is used to achieve an overall speedup of 10?

(b) Assume the distribution of enhancement usage is 30%, 30%, and 20% for E1, E2, and E3, respectively. Assuming all three enhancements are in use, for what fraction of the reduced execution time is no enhancement in use?

3.

(i) Describe briefly about the pipeline concept of the computer architecture.

(ii) What is meant by *Speedup*?

(iii) State an equation for the *speedup* (S) using following information.

n = number of instructions, t_n = non-pipeline time to complete each instruction,

k = number of segments, t_p = clock cycle time for a pipeline.

(iv) Consider the following two systems.

System A: a non-pipelined system that needs 30 ns to complete an instruction,
System B: a system with 5 pipeline stages.

(a) If the pipeline segments take 10, 8, 12, 15, and 11 ns to complete their work, what is t_p ? Explain your answer.

(b) How long will each system take to compute 10,000 instructions? (Assume there are no branches.)

(c) What is the speedup for 10,000 instructions? (Assume there are no branches.)

(d) If there were branches, how would this affect your answers above?

4.

(i) An alternative to sharing L2 cache among the processors is to partition the L2 cache into multiple private L2 caches, one for each processor.

(a) Describe two advantages of having a shared L2 cache, instead of private L2 caches.

(b) Describe at least two advantages of having private L2 caches for each processor, instead of a shared L2 cache.

(ii) Describe and distinguish between the Cache Addressing and Virtual Memory page Addressing.

(iii) Consider a memory system with a capacity of 2^{32} bytes. The processor system has a 4096-byte cache with 32-byte block size. For the following two cache organizations, determine how many bits are used for tag, index, and block offset.

(a) 4-way set-associative (b) 32-way set-associative

5.

(i) Briefly explain the importance of Instruction Set Architecture (ISA) in CPU Design.

(ii) Consider the following arithmetic expression:

$$Y = ((A*B) - (C/D))/ (D + (E*F)),$$

Where "*" and "/" represents multiplication and division respectively.

The integer variables A, B, C, D, E and F are stored in consecutive memory locations starting from memory address 1000H and each takes 4 bytes.

(a) Write Reverse Polish Notation of the given expression.

(b) Write the sequence of required assembly level instructions that would implement the above expression in stack-based CPU.

Assume that the availability of the instructions as MOV, POP, PUSH, ADD, SUB, DIV and MUL.

SUB: TOS ← (TOS) – (SOS),
DIV: TOS ← (TOS)/ (SOS)
; Where TOS: Top of Stack, SOS: Second of Stack

6. A simple analogue to digital converter (SADC) is interfaced to a PC via parallel port (Appendix A) or ISA bus (Appendix B) to measure analogue signals. SADC operates as follows.

When the PC sets the SOC (Start of Conversion) signal then SADC read the input analogue signal and start the conversion. After conversion completed, SADC sets the interrupt signal EOC (End of Conversion) which will be sent to PC to indicate the end of the operation.

Digital equivalent (D) of analogue signal is inversely proportional to the time (T seconds) between SOC and EOC signals. Hence, digital equivalent can be computed as D = 2K/T (where "K" is a predefined constant), and the width is 8 bits.

(i) Draw a block diagram to show the connectivity of the device with the computer through the parallel port (Appendix A) or ISA bus (Appendix B). Clearly indicate address, data and control signals that involve and the pins of parallel port or ISA Bus.

(ii) Draw a typical timing diagram for reading data from the SADC.

(iii) Give an algorithm to compute digital equivalent. You must show all value used for configuring the ISA bus (data and address) or the parallel port (data and address of relevant ports).

(iv) Explain how to use a Logic Analyzer for timing analysis with the help of your block diagram. Clearly indicate address, data and control signals that involve and the pins of parallel port or ISA Bus.

7.

(i) Briefly describe the advantage of Redundant Array of Inexpensive Disk (RAID).

(ii) Describe the Asynchronous and Synchronous methods of communication between two devices.

(iii) Briefly describe the following I/O control systems: Programmed I/O, Interrupt I/O and Coprocessor I/O.

(iv) Consider a processor with Programmed I/O that executes instruction at a rate of 0.1 MIPS. An I/O subroutine for writing to disk requires 10,000 instructions and the disk has total latency of 100ms. What is the suspended time of the main program?

8.

(i) Describe the Flynn's classification (SISD, SIMD, MISD, and MIMD) on computer organization giving block diagrams for each organization.

(ii) Distinguish MIMD multiprocessors from multi-computers or computer networks.

(iii) What are the salient features of RISC architecture and CISC architecture? Provide advantages and disadvantages of each architecture.

(iv) A processor executes 10 million floating point and one million overhead instructions in 50ms. What is the MFLOPS rating of this processor? What would be the MIPS rating of the same processor.

Appendix A

Parallel port connector description

Pin: D-sub	Signal	Function	Source	Register		Inverted at con-nector?	Pin: Centron-ics
				Name	Bit #		
1	nStrobe	Strobe D0-D7	PC[1]	Control	0	Y	1
2	D0	Data Bit 0	PC[2]	Data	0	N	2
3	D1	Data Bit 1	PC[2]	Data	1	N	3
4	D2	Data Bit 2	PC[2]	Data	2	N	4
5	D3	Data Bit 3	PC[2]	Data	3	N	5
6	D4	Data Bit 4	PC[2]	Data	4	N	6
7	D5	Data Bit 5	PC[2]	Data	5	N	7
8	D6	Data Bit 6	PC[2]	Data	6	N	8
9	D7	Data Bit 7	PC[2]	Data	7	N	9
10	nAck	Acknowledge (may trigger interrupt)	Printer	Status	6	N	10
11	Busy	Printer busy	Printer	Status	7	Y	11
12	PaperEnd	Paper end, empty (out of paper)	Printer	Status	5	N	12
13	Select	Printer selected (on line)	Printer	Status	4	N	13
14	nAutoLF	Generate automatic line feeds after carriage returns	PC[1]	Control	1	Y	14
15	nError (nFault)	Error	Printer	Status	3	N	32
16	nInit	Initialize printer (Reset)	PC[1]	Control	2	N	31
17	nSelectIn	Select printer (Place on line)	PC[1]	Control	3	Y	36
18	Gnd	Ground return for nStrobe, D0					19,20
19	Gnd	Ground return for D1, D2					21,22
20	Gnd	Ground return for D3, D4					23,24
21	Gnd	Ground return for D5, D6					25,26
22	Gnd	Ground return for D7, nAck					27,28
23	Gnd	Ground return for nSelectIn					33
24	Gnd	Ground return for Busy					29
25	Gnd	Ground return for nInit					30
	Chassis	Chassis ground					17
	NC	No connection					15,18,34
	NC	Signal ground					16
	NC	+5V	Printer				35

[1]Setting this bit high allows it to be used as an input (SPP only) [2]Some Data ports are bidirectional.

Parallel port register definitions

Base address: 0378h

Data Register (Base Address)

Bit	*Pin: D-sub*	Signal Name	Source	Inverted at connector?	Pin: Centroni
0	2	Data bit 0	PC	no	2
1	3	Data bit 1	PC	no	3
2	4	Data bit 2	PC	no	4
3	5	Data bit 3	PC	no	5
4	6	Data bit 4	PC	no	6
5	7	Data bit 5	PC	no	7
6	8	Data bit 6	PC	no	8
7	9	Data bit 7	PC	no	9

Some Data ports are bidirectional. (See Control register, bit 5 below.)

Status Register (Base Address +1)

Bit	*Pin: D-sub*	Signal Name	Source	Inverted at connector?	Pin: Centroni
3	15	nError (nFault)	Peripheral	no	32
4	13	Select	Peripheral	no	13
5	12	PaperEnd	Peripheral	no	12
6	10	nAck	Peripheral	no	10
7	11	Busy	Peripheral	yes	11

Additional bits not available at the connector:
0: may indicate timeout (1=timeout).
1, 2: unused

Control Register (Base Address +2)

Bit	*Pin: D-sub*	Signal Name	Source	Inverted at connector?	Pin: Centroni
0	1	nStrobe	PC[1]	yes	1
1	14	nAutoLF	PC[1]	yes	14
2	16	nInit	PC[1]	no	31
3	17	nSelectIn	PC[1]	yes	36

[1]When high, PC can read external input (SPP only).
Additional bits not available at the connector:
4: Interrupt enable. 1=IRQs pass from *nAck* to system's interrupt controller. 0=IRQs do not pass to interrupt controller.
5: Direction control for bidirectional Data ports. 0=outputs enabled. 1=outputs disabled; Data port can read external logic voltages.
6,7: unused

Appendix B

ISA (Industry Standard Architecture) Bus

Pins layout

D	Description	Name	Pin	Pin	Name	Description	D
/	Ground	GND	B1	A1	IO CHK	I/O Channel Check	-I
O	Reset	RESET	B2	A2	SD7	System Data bit 7	I/O
/	Power +5V	+5V	B3	A3	SD6	System Data bit 6	I/O
I	Interrupt Request 9	IRQ9	B4	A4	SD5	System Data bit 5	I/O
/	Power -5V	-5V	B5	A5	SD4	System Data bit 4	I/O
I	DMA Request 2	DRQ2	B6	A6	SD3	System Data bit 3	I/O
/	Power -12V	-12V	B7	A7	SD2	System Data bit 2	I/O
/	Zero Wait State	0WS	B8	A8	SD1	System Data bit 1	I/O
/	Power +12V	+12V	B9	A9	SD0	System Data bit 0	I/O
/	Ground	GND	B10	A10	IO RDY	I/0 Channel Ready	-I
O	System Memory Write	SMEMW	B11	A11	AEN	Address Enable	O
O	System Memory Read	SMEMR	B12	A12	SA19	System Address bit 19	O
I/O	I/O Write	IOW	B13	A13	SA18	System Address bit 18	O
I/O	I/O Read	IOR	B14	A14	SA17	System Address bit 17	O
O	DMA Request Acknowledge 3	DACK3	B15	A15	SA16	System Address bit 16	O
I	DMA Request 3	DRQ3	B16	A16	SA15	System Address bit 15	O
O	DMA Request Acknowledge 1	DACK1	B17	A17	SA14	System Address bit 14	O
I	DMA Request 1	DRQ1	B18	A18	SA13	System Address bit 13	O
I/O	Refresh cycle in progress	REFRESH	B19	A19	SA12	System Address bit 12	O
O	System Clock	CLOCK	B20	A20	SA11	System Address bit 11	O
I	Interrupt Request 7	IRQ7	B21	A21	SA10	System Address bit 10	O
I	Interrupt Request 6	IRQ6	B22	A22	SA9	System Address bit 9	O
I	Interrupt Request 5	IRQ5	B23	A23	SA8	System Address bit 8	O
I	Interrupt Request 4	IRQ4	B24	A24	SA7	System Address bit 7	O
I	Interrupt Request 3	IRQ3	B25	A25	SA6	System Address bit 6	O
O	DMA Request Acknowledge 2	DACK2	B26	A26	SA5	System Address bit 5	O
O	T/C	TC	B27	A27	SA4	System Address bit 4	O
?	Buffered Address Latch Enable	BALE	B28	A28	SA3	System Address bit 3	O
/	Power +5V	+5V	B29	A29	SA2	System Address bit 2	O
O	Oscillator	OSC	B30	A30	SA1	System Address bit 1	O
/	Ground	GND	B31	A31	SA0	System Address bit 0	O

Signal Description

CLOCK (*System Drive*) output
The system clock is a synchronous microprocessor cycle clock.

RESET (*Reset Drive*) output
This signal goes high at power-up, hardware reset, or when low line-voltage occurs.

SA0 to SA19 (*System Addresses*) input/output
The system address lines run from bit 0 through 19. They are latched onto the falling edge of BALE.

SD0 to SD7 (*System Data bits*) Input/Output
System data bits 0 to 7.

BALE (*Buffered Address Latch Enable*) input
The buffered address latch enable is used in latch SA0 to SA19 on the falling edge of BALE. During DMA cycles, BALE is forced high.

IO CHK (*I/O Channel Check*) active low input
I/O channel check is active low signal which indicate that a parity error exists in the I/O board.

IO RDY (*I/O Channel Ready*) input
This signal lengthens I/O or memory cycles and should be held low with valid addresses. It can be held low for a maximum of 2.5 microseconds.

IRQ 3 to 7, 9 (*Interrupt Requests*) input
These interrupt request signals indicate I/O service request attention. They are prioritized in the following sequences: highest IRQ 9 and lowest IRQ 3, 4, 5,6,7,8.

IOR (*I/O Read*) active low input/output
Instructs an I/O device to drive its data onto the data bus.

IOW (*I/O Write*) active low output
Instructs an I/O device to read the data off the data bus.

SMEMR (*System Memory Read*) output
The system memory read signal is low while the low first megabyte memory is being read.

SMEMW (*System Memory Write*) output
The system memory write signal is low while the low first megabyte memory is being written.

DRQ 0 to 3 (*DMA Requests*) active high input
DMA Request channels 0 to 3 are for 8-bit data transfers. DRQ4 is used on the system board. Hold a DRQ line high until its DMA Request Acknowledge (DACK) goes active. Their priority is in the following sequences: highest DRQ 0,1,2, and 3.

DACK 1 to 3 (*DMA Request Acknowledges*) output
These signals are used to acknowledge the corresponding signals for DRQ 0 to 3.

AEN (*Address Enable*) output
The address enable is high when the DMA controller drives the address bus and is low when the CPU drives the address bus.

REFRESH (*Refresh cycle in progress*) active low input/output
This signal indicates a refresh cycle is in progress.

TC (*T/C*) output

OSC (*Oscillator*) output
The oscillator signal is used for the color graphic card.
High-speed clock (70 ns, 14.31818 MHz), 50%duty cycle

0WS (*Zero Wait State*) input
The zero wait state indicates to the microprocessor that the present bus cycle can be completed without inserting any additional wait cycles.