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The Open University of Sri Lanka
Department of Electrical and Computer Engineering
Final Examination –2010

ECX5330 – **Electronic systems** **(Closed Book)**

Time: 1400-1700 hrs. Date: 01.04.2011

Answer any five questions.

1. The op-amp circuits shown in Figure-Q1(a) and Figure-Q1(b) use non linear feedback. The bipolar transistors used in both circuits are matched.

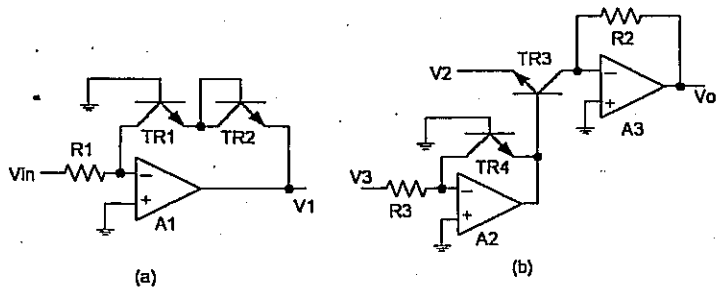


Figure-Q1

(i) Derive an expression for V_1 in Figure-Q1(a).

(ii) Show that Vo represents antilogarithm of V_2 in Figure-Q1(b).

(iii) Use these two circuits to form a circuit which will have the relationship $Vo = k(Vin)^2$ where k is a constant. Derive an expression for k and evaluate the required circuit parameters for $k = 1000$ when Vin and Vo are in volts.
R1 = 1k R2 = 100k R3 = 10k

(iv) If the amplifier A1 has an input offset voltage of 1mV and an input bias current of 200nA, calculate the percentage error at the output when Vin = 20mV. Neglect the effect of offset errors in A2 and A3 on Vo.

2. A multistage amplifier with an external feedback is shown in figure-Q2. The first stage is a transresistance amplifier having open loop gain A_R while the second stage is a voltage amplifier having open loop gain A_V. The input and the output impedance of the stages are R1, R2, R3 and R4 while the signal source is represented with V_S and R_S.

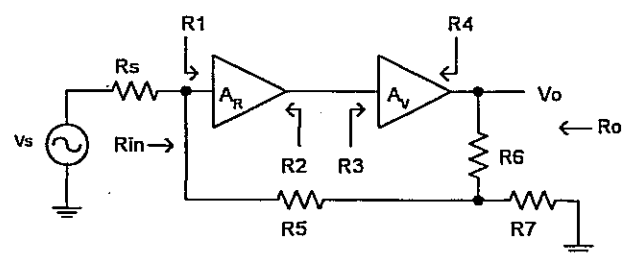


Figure-Q2

(i) Identify the type of feedback and draw the open loop ac equivalent circuit considering the loading effects of the feedback network.

(ii) Find expressions for the feedback factor and the open loop gain in (a) with respect to the feedback topology used.

(iii) Calculate the open loop gain and the feedback factor. Hence calculate the closed loop voltage gain, input impedance and the output impedance applying feedback principles.

$A_R = -50V/A$ $A_V = 50$ R1 =1k R2 = 500Ω
R3 = 1.5k R4 = 200Ω R5 = 2k R6 = 100k
R7 = 1k R_S = 1k

(iv) Assuming that the open loop amplifier is having a dominant pole and the closed loop bandwidth of 1MHz, find out the pole frequency and the gain crossover frequency of the open loop amplifier.

3. A constant current source and an application of it are shown in Figure-Q3. Assume that the transistors are identical and of high gain.

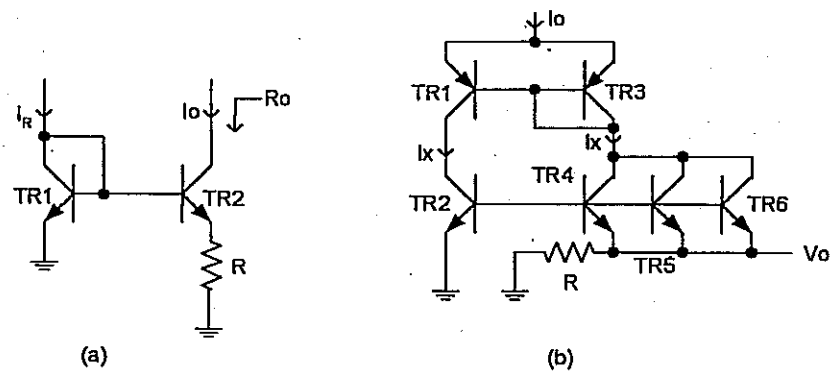


Figure-Q3

(i) Find an expression for R in Figure-Q3(a) and calculate its value assuming, $I_R = 1mA$ $I_O = 0.1mA$ $V_T = 25mV$ at the room temperature

(ii) Find an expression for the dynamic resistance R_O in the Figure-Q3(a). Let the collector-emitter resistance and the base-emitter resistance is given by r_o and r_π.

(iii) Show that the voltage V_O in Figure-Q3(b) is proportional to the absolute temperature evaluating the constant of proportion. Note that the bases of the transistors TR2, TR4, TR5 and TR6 are connected together.

Boltzmann constant $K = 1.38 \times 10^{-23} J/^0 K$

Charge of an electron $q = 1.6 \times 10^{-19} Coulombs$

4. A two stage amplifier has a voltage gain 10^4 with poles at 10^6, 10^7 and 10^8.

(i) Write the open loop gain function $H(\varpi)$ and find the open loop bandwidth.

(ii) Draw the gain and the phase Bode plots with labeled axis.

(iii) Find the range of usable closed loop gain to have a phase margin not less than 45^0. Also find the maximum possible bandwidth, the closed loop

gain, the gain margin and the feedback factor associated with this condition.

(iv) It is required to use this amplifier with a feedback factor of 0.1 and with a phase margin of 45^0. Employing lag-lead compensation to achieve this, show the compensation network and find the values of the components. Any capacitors used must not exceed 1nF.

5. A circuit of a band pass filter is shown in Figure-Q5. The operational amplifier can be assumed as ideal and K is a constant.

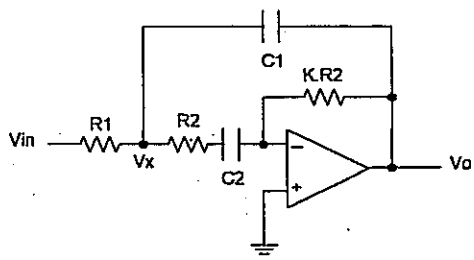


Figure-Q5

(i) Derive the transfer function $H(s)$ of the circuit.

(ii) Considering the standard function of a band pass filter $\dfrac{H\left(\dfrac{\varpi_0}{Q}\right)s}{s^2+\left(\dfrac{\varpi_0}{Q}\right)s+\varpi_0{}^2}$, show that the bandwidth B is given by $B=\dfrac{\varpi_0}{Q}$.

(iii) Design a band pass filter using this circuit for a center frequency of 200Hz with a bandwidth of 20Hz. What is the pass band gain of your filter? You may assume R1=R2 and C1=C2. Use capacitor values not less than 0.1μF.

6. An amplifier using BJT transistors is shown in Figure-Q6.

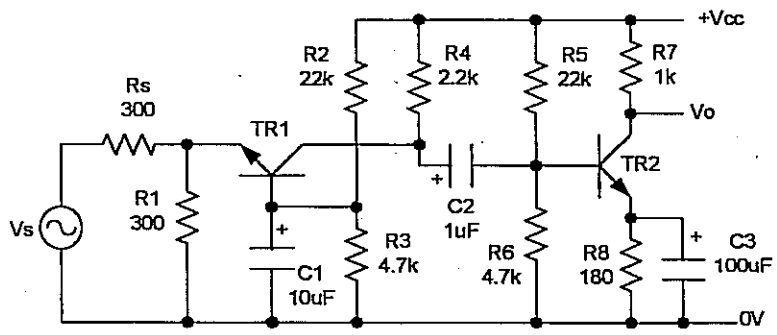


Figure-Q6

The input signal source is denoted by Vs and Rs. You may neglect the effects of the coupling capacitors.

(i) Draw the high frequency equivalent circuit using hybrid-π model of the transistors. Assume that the transistors are identical and $r_{bb'} = 0$.

(ii) Derive the multi pole voltage gain transfer function at high frequencies using $R_a = R_1 // r_{b'e}$ and $R_b = R_4 // R_5 // R_6$.

(iii) Calculate the mid band gain, the pole frequencies and the upper 3dB cut-off frequency.

$g_m = 20\frac{mA}{V}$ $\quad r_{b'e} = 5k$ $\quad r_{bb'} = 0$ $\quad r_{ce} = \infty$

$c_{b'e} = 5pF$ $\quad c_{b'c} = 2pF$

7. (a) Draw the block diagram of a successive approximation type analog to digital converter (ADC) identifying the blocks. Find expressions for the maximum frequency of the sampling clock and the register clock using the propagation delays associated with various blocks. You may neglect any delays in the control circuits. Assume that the number of bits in the register is 'n'.

(b) A successive approximation type ADC has an 8 bit register and a reference voltage of 2.5V.

(i) Find the resolution of this ADC in mV. Determine the digital output for an input voltage of 1.453V. Tabulate the conversion sequence for this input showing the register contents and the digital output with the register clock.

(ii) Calculate the minimum value of the hold capacitor in order to have capacitor voltage droop within $\pm\frac{1}{2}LSB$ during a conversion. The input bias current of the comparator is 3μA and the sampling clock is 450 kHz.

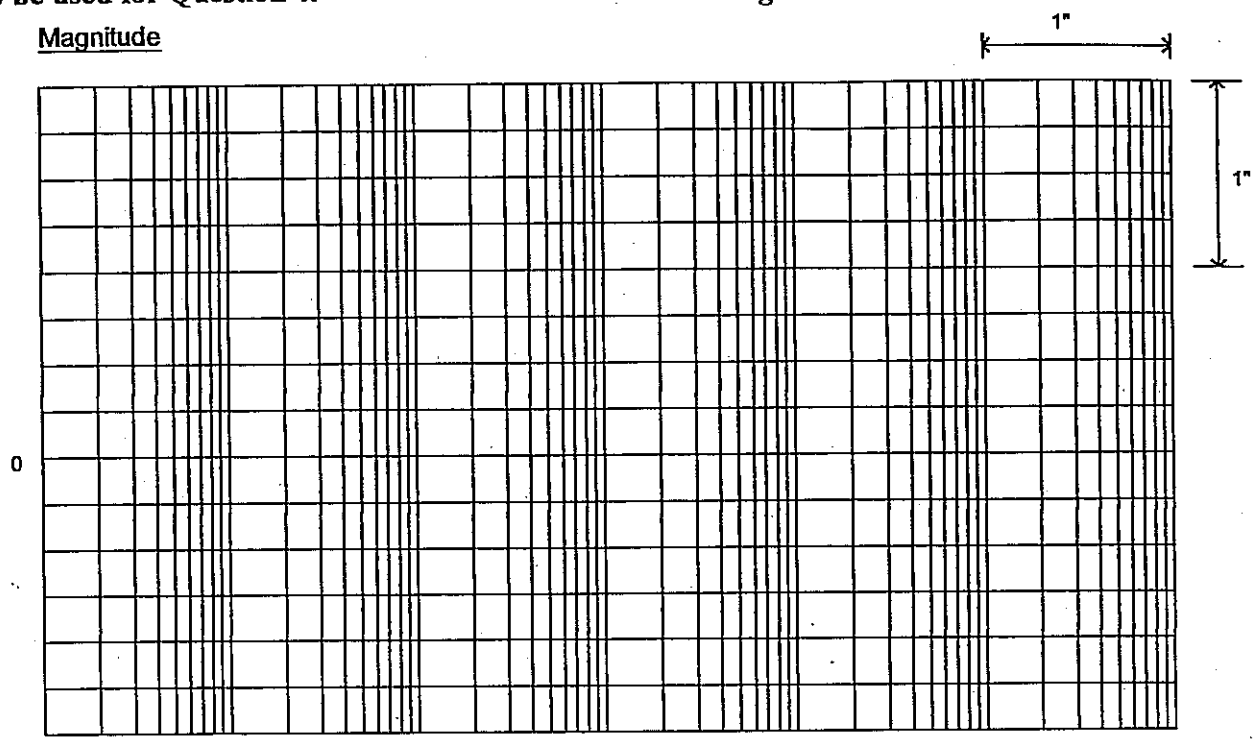
8. (a) Draw the block diagram of a 8 input multiplexer. Implement the function f = Σ 0, 1, 2, 3, 5, 7, 10, 11 using a 8 input multiplexer with the aid of basic gates.

(b) (i) Complete the following output sequence of a shift register.
0, -, 2, -, 3, -, 6, -, 0

(ii) Design a sequence generator to generate the binary sequence 10110101 using a shift register with the aid of basic gates. Show the steps of your design clearly.

To be used for Question 4. **Reg. No:**

Magnitude



Phase

