THE OPEN UNIVERSITY OF SRI LANKA
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

FINAL EXAMINATION - 2012/2013

ECX6330 – ELECTRONIC SYSTEMS **(Closed Book)**

ANSWER ANY FIVE QUESTIONS.

Date 21.08.2013 ***Time: 9:30-12:30 hrs.***

Q1. Consider the circuit in the Figure-Q1.

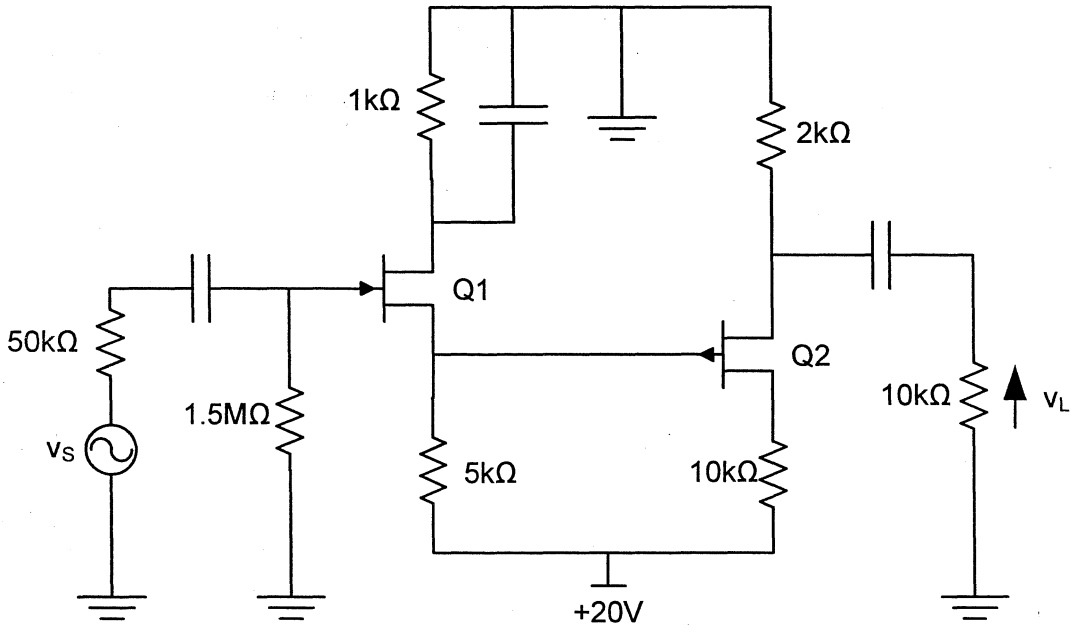


Figure-Q1

Assume that $r_{d1} = r_{d2} \rightarrow \infty$, $g_m = 1.6\ mAV^{-1}$ for both Q1 and Q2.

(a) Draw the low frequency equivalent circuit. **(6Marks)**

Hence find,

(b) Input impedance. **(4Marks)**

(c) Output impedance. **(4Marks)**

(d) Mid band voltage gain $\frac{V_L}{V_S}$. **(6Marks)**

Q2. Let the transistor in the amplifier circuit in Figure-Q2 has the following parameters with the usual notation. $r_{be} = 1k\Omega, r_{bc} = 4M\Omega,\ r_{ce} = 80k\Omega,\ C_c = 3pF,\ C_e = 100pF$ and $g_m = 50mAV^{-1}$.

Assume the effect of all the other unmentioned parameters to be negligible.

(a) Draw the high frequency equivalent circuit for this amplifier circuit. **(6Marks)**

(b) Using Miller's theorem, simplify the equivalent circuit model. **(6Marks)**

(c) Hence, find the voltage gain of the same amplifier. **(8Marks)**

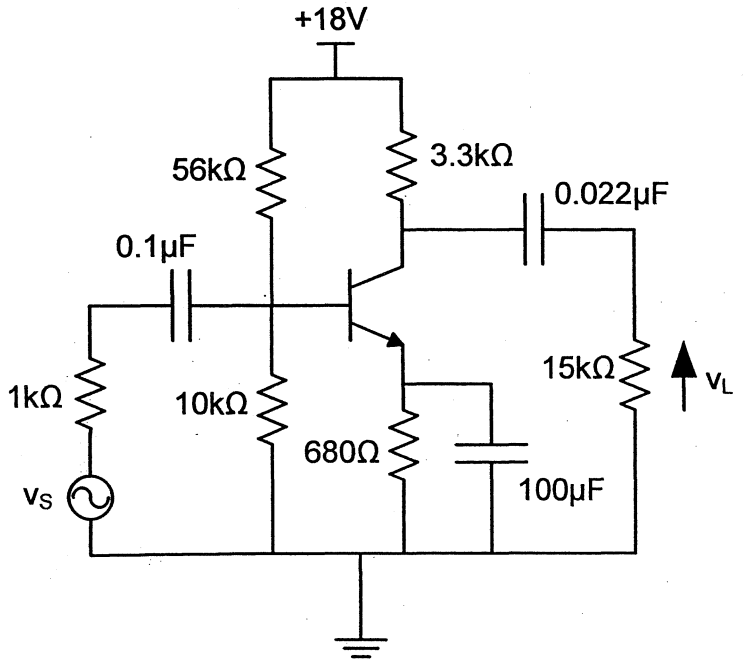


Figure-Q2

Q3.

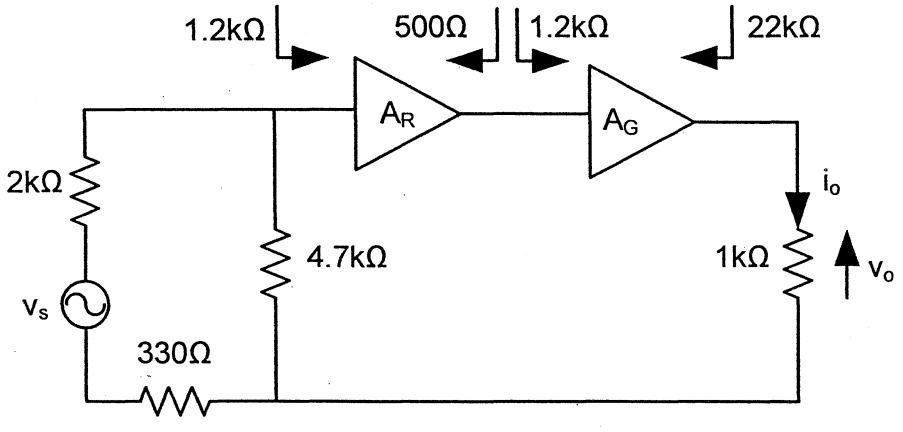


Figure-Q3

The circuit shown in the above Figure-Q3 has a transresistance amplifier and a transconductance amplifier with $A_R = -100\ VA^{-1}$ and $A_G = 50\ AV^{-1}$ respectively.

The input and output impedances of the two amplifier stages are as shown.

(a) Draw the open loop ac equivalent circuit. **(6Marks)**

(b) Find the open loop gain and the feedback factor. **(8Marks)**

(c) Hence find the closed loop current gain, input impedance and the output impedance. **(6Marks)**

Q4.

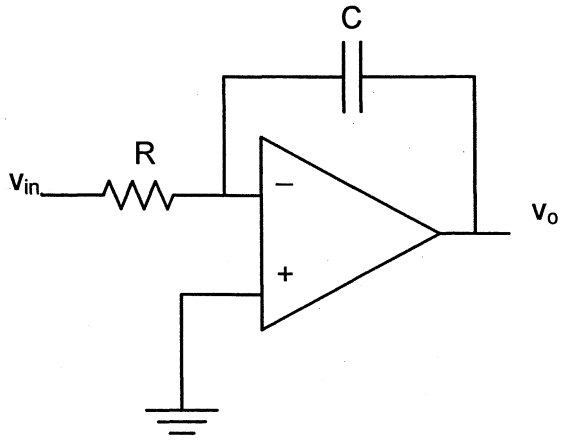


Figure-Q4

(a) Assuming an ideal operational amplifier except a finite gain, derive the voltage gain transfer function of the above circuit in Figure-Q4. **(4Marks)**

(b) Hence, sketch the magnitude and phase Bode plots. Plot the magnitude and phase Bode plots for an all ideal operational amplifier in the same sketch. (Clear axis labeling and plots are required. Assume $R = 1.6k\Omega$ and $C = 0.01\mu F$) **(8Marks)**

(c) If this operational amplifier is a real dominant pole amplifier with a low frequency gain of 60dB and a pole at 100Hz, determine the usable frequency range of the above circuit. **(8Marks)**

Q5.

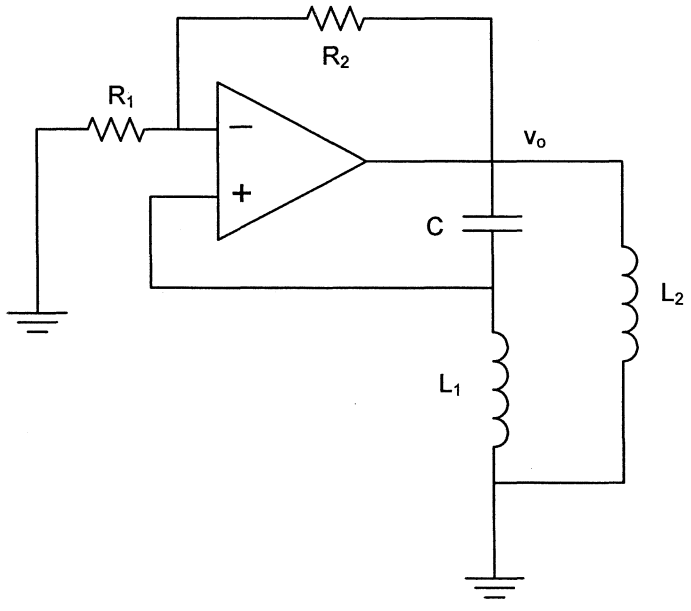


Figure-Q5

(a) Starting from the first principles, derive the Barkhousen criteria for oscillations to occur. **(4Marks)**

(b) Stating all your assumptions, derive an expression for the feedback factor for the circuit in Figure- Q5. **(8Marks)**

(c) Derive an expression for the forward gain. **(2Marks)**

(d) Hence find the frequency of oscillation. **(6Marks)**

Q6.

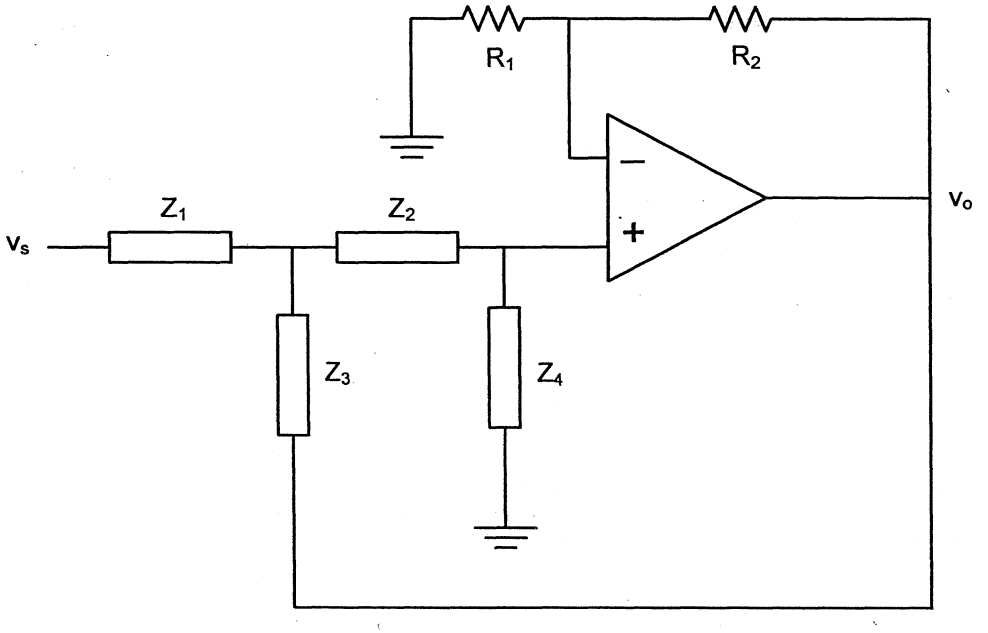


Figure-Q6

(a) Derive the transfer function of the active filter circuit shown in Figure-Q6. **(4Marks)**

(b) Hence find the components required to have a second order high-pass filter. **(6Marks)**

(c) Using the results of (a) and (b), deduce the component values required for a cutoff frequency of 200kHz. (You may simplify the calculation with assumptions. State all your assumptions clearly) **(4Marks)**

(d) Calculate the pass band gain of your designed filter. **(6Marks)**

Q7.

(a) A weight measuring system should measure $500 - 2500kg$ with a resolution of at least $10kg$. Sensitivity of the transducer employed is $5mVkg^{-1}$. The output of the transducer is fed to an ADC. Calculate the minimum number of bits required at the ADC and the minimum possible resolution at the ADC input. **(6Marks)**

(b) An inexperienced driver needs to park his car outside his apartment complex in a 5 slotted car park. The driver prefers to have three adjacent slots to be available. He has mounted sensors to monitor each parking slot where a sensor will output logic 0 when a slot is vacant. Design a circuit which will accept the sensor outputs as inputs and then outputs logic 1 whenever three adjacent slots or two edge slots are available. (Note: This driver is capable of parking at the edge of the park with even when only 2 slots are available).

i. State the truth table. **(4Marks)**
ii. Use a Karnough map to produce a simplified Boolean expression. **(4Marks)**
iii. Produce the logic circuit with a PLD. **(6Marks)**

Q8.

(a) Design a synchronous counter to produce a sequence $\mathbf{0 \rightarrow 5 \rightarrow 10 \rightarrow 15 \rightarrow 0.}$ **(6Marks)**

(b) Design an asynchronous counter to produce the same sequence as in (a). **(6Marks)**

(c) Design a sequential circuit to detect ***1001*** in a long sequence of bits. (Consider overlaps) **(8Marks)**