THE OPEN UNIVERSITY OF SRI LANKA
FACULTY OF ENGINEERING TECHNOLOGY
DIPLOMA IN TECHNOLOGY – LEVEL 3
FINAL EXAMINATION 2008/2009

MEX3272 – APPLIED ELECTRONICS

DATE	:	**17th MARCH 2009**
TIME	:	**0930 HRS. – 1230 HRS.**
DURATION	:	**THREE (03) HOURS**

C48

INSTRUCTIONS

- *Question paper consists of **eight** questions. Answer **only five** questions.*
- *All questions carry equal marks.*

Question 01

(a) State the Thevenin's theorem and Norton's theorem.

(b) i. The Thevenin equivalent circuit of a network consists of a voltage of 9 V in series with an impedance of 2 Ω. Find the Norton equivalent of circuit.

ii. The Norton equivalent circuit of a network consists of a current of 12 A in parallel with an impedance of 3 Ω. Find the Thevenin equivalent of circuit.

(c) Following Figure Q1(c) represents an active network consisting of two voltage sources and four linear resistors. Find the

i. Thevenin equivalent circuit,
ii. Norton equivalent circuit, at terminal **A** and **B**.

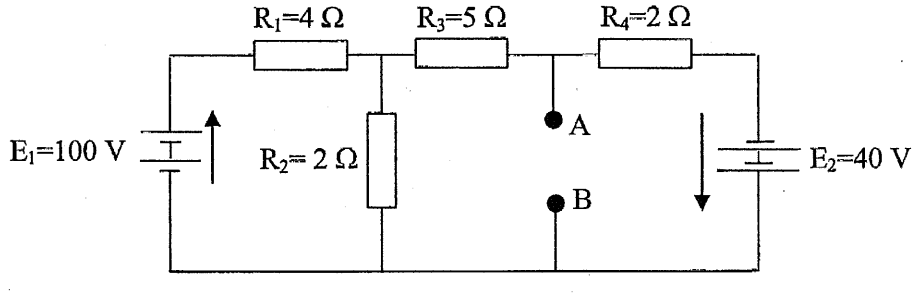


Figure Q1(c)

(d) Following Figure Q1 (d) shows a commercial Wheatstone bridge, R_1 is a fixed 1 kΩ resistor, R_3 can be adjusted in 1Ω steps from 0 to 1100Ω, and R_2 can be selected to be 1 kΩ, 10 kΩ, 100 kΩ or 1 MΩ

i. Suppose that the bridge is balanced with R_3= 732 Ω and R_2 =10kΩ. What is the value of R_x?
ii. What is the largest value of R_x which the bridge can be balanced?
iii. Suppose that R_2 =1 MΩ. What is the increment between values of R_x for which the bridge can be precisely balanced?

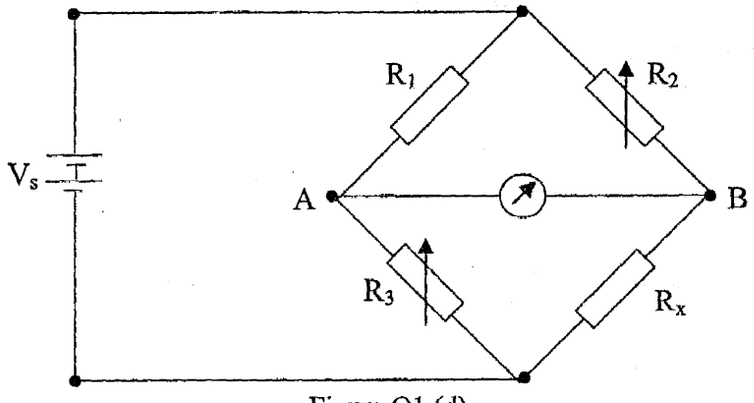


Figure Q1 (d)

Question 02

(a) Describe the gain-versus-frequency responses of the basic filters as low-pass, high-pass, band-pass and band-stop.

(b) Determine the center frequency, bandwidth, quality factor and damping factor of a band-pass filter.

(c) Describe the three basic filter response characteristics.

(d) Consider the circuit given in the Figure Q4 (d).

i. Identify the filter.
ii. Determine center frequency, maximum gain and bandwidth.

Where; R_1 = 68 kΩ , R_2=180 kΩ , R_3=2.7 kΩ and $C_1 = C_2$ = 0.01μF.

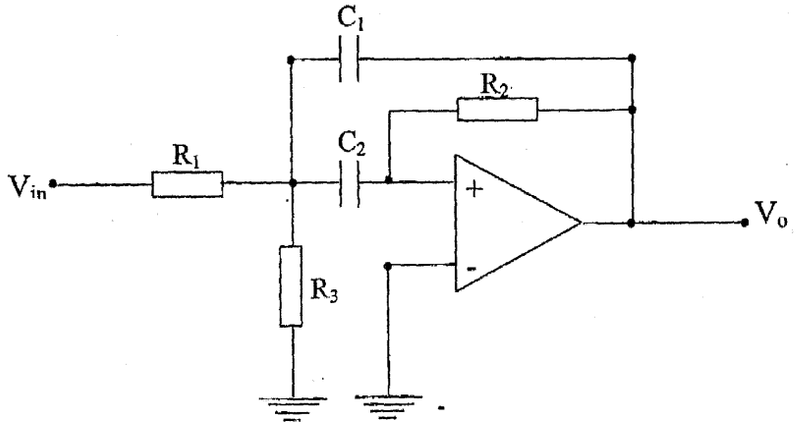


Figure Q2 (d)

Question 03

(a) Draw a circuit symbol and characteristics of a diode.

(b) What are the half wave and full wave rectification methods, explain it using circuit diagrams.

(c) Draw a circuit symbol and V-I characteristics of a typical zener diode.

(d) The load resistance R_L in the voltage regulator circuit of Figure Q3 (d) is fixed at 10kΩ. But the input supply voltage V_I varies from 80 V to 120 V.

i. Does zener remain "on" even when the input supply voltage reduces to 80 V?
ii. Calculate the maximum value of zener diode current.
iii. Calculate the minimum value of zener diode current.

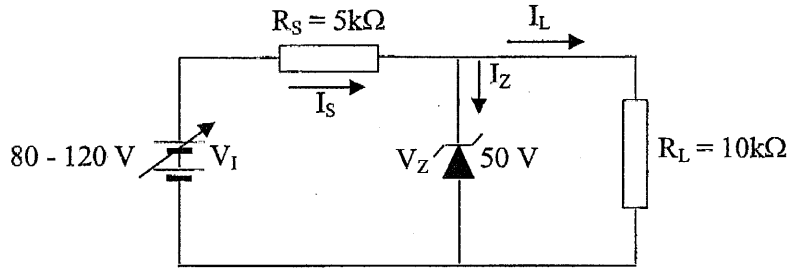


Figure Q3 (d)

Question 04

(a) What are the types of Field Effect Transistor (**FET**)?

(b) The JFET equation is given by $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

i. What is the physical significance of I_{DSS} and V_P?
ii. For what range of values of I_D and V_{GS} does the equation apply?

(c) A JFET have following data under test,

$V_{GS} = -2V$	$I_D = 5$ mA
$V_{GS} = -3V$	$I_D = 1.25$ mA

Determine I_{DSS} and V_P.

(d) Find the bias levels for the circuit shown in Figure Q4 (d).Given that I_{DSS}=10 mA, $V_{GS(off)} = V_P = 3$ V, $V_{DD} = -10$ V ,$R_1 = 90k\Omega$, $R_2 = 10k\Omega$, $R_D = 2k\Omega$ and $R_S = 1k\Omega$

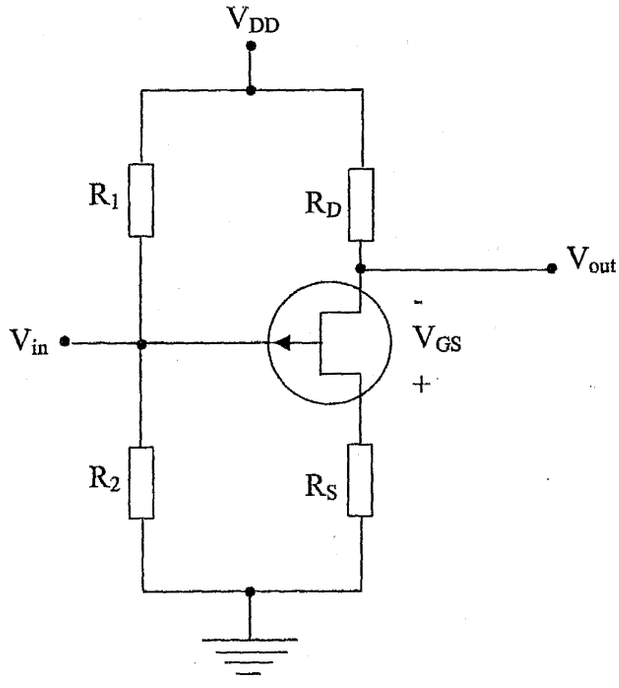


Figure Q4 (d)

Question 05

(a) Give four characteristics of an ideal operational amplifier (Op-Amp) and compare the ideal values with its typical values.

(b) Explain following terms of an operational amplifier

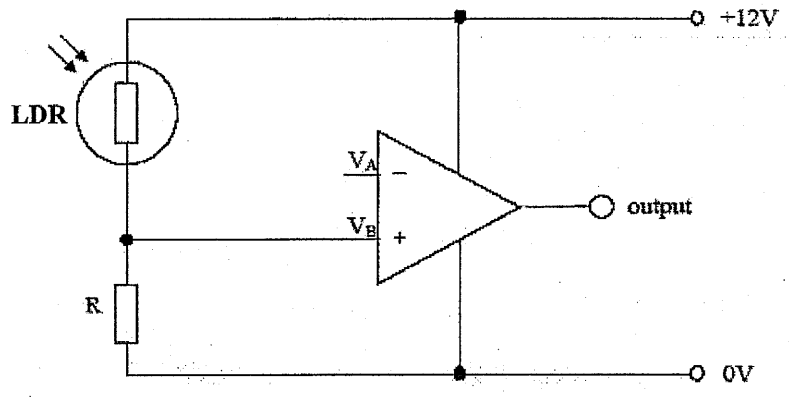
i. Input off set current
ii. Output offset voltage
iii. Common Mode Rejection Ratio (**CMRR**)
iv. Slew rate.

(c)

i. What is a voltage follower? Explain it using a circuit diagram and find the voltage gain of it?

ii. Design a circuit that gives ±9V using following component and device.
Two Op-Amps, +12V voltage source, one 3 kΩ, one 9 kΩ and two 10 kΩ resistors.

(d) A light sensor subsystem connected to part of a comparator circuit is shown in Figure Q5 (d).



The op-amp input V_A requires a reference voltage of 6 V.

i. Draw a voltage divider connected to the circuit to show how this is achieved (Select suitable values).

ii. The LDR has a resistance of 10 kΩ at a certain light level. Calculate the value of **R** required to make the comparator switch at this light level, explain your working.

The LDR data sheet gives its resistance at two light levels.

Light level (lux)	**Typical resistance (kΩ)**
5	20
100	5

iii. Give the output voltage from the op-amp at
(1) 100 lux
(2) 5 lux.

Question 06

Explain only five terms using diagrams and mention one application for each of them.

i. SCR
ii. LDR
iii. Opto coupler
iv. Thermo couple
v. Successive Approximation Converter
vi. Dual Slope Integrating Converter
vii. Flash Converter

Question 07

(a) i. Convert 10011101_2 to Octal and Hexadecimal

ii. Express the decimal number -39 in

a. Sign magnitude method
b. 1's compliment method
c. 2's compliment method

(b) i. State De Morgan's theorem for three Boolean variables A, B and C.

ii. Define the following 2-input device.

a. OR gate
b. NAND gate
c. Exclusive NOR gate

iii. Realize an Exclusive OR gate using only NAND gates.

(c)

i. Show that,

$$A + A\overline{B} = A + B$$

ii. Simplify the following logic functions using Boolean algebra.

1. $[A\overline{B}(C + BD) + \overline{A\overline{B}}]C$
2. $\overline{A}BC + A\overline{B}\overline{C} + \overline{A}\overline{B}\overline{C} + A\overline{B}C + ABC$

(d) A, B, C, D are four inputs of a circuit, representing binary values from 0000 to 1111 (i.e. 0 to 15). The input A is MSB and D is LSB. The out put of the circuit (F) is **true**, if the input is divisible by 2, 3, 5 or 7 with the exception of 15, otherwise the output is **false.** Assume that zero is not divisible by any number.

i. Write the Boolean expression for the output (F) and simplify it using Karnaugh map, Show the steps very clearly.
ii. Design a circuit using logic gates (OR, AND and NOT) to carry out the function.

Question 08

(a) Explain briefly the terms "Combinational-logic" and "Sequential-logic".

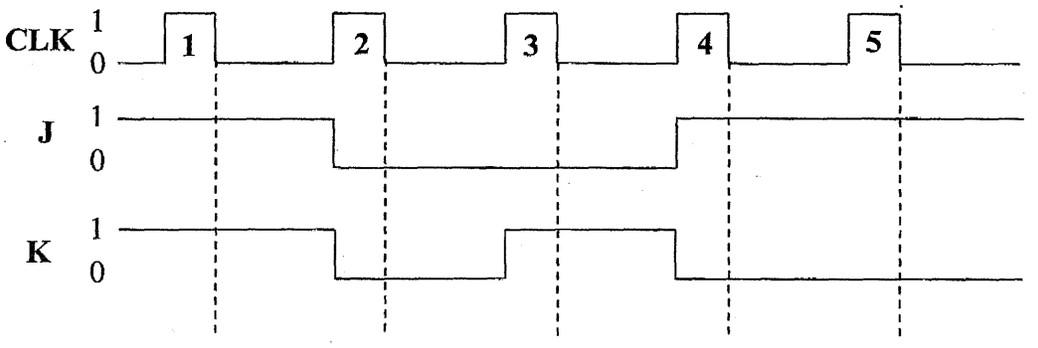
(b) Explain:

i. Propagation delay
ii. Synchronous operation
iii. Asynchronous operation
iv. Set-up time
v. Hold time

(c)

i. Discuss the operation of **J-K**, **S-R** and **D** edge-triggered flip-flop. (Give circuit diagrams, truth tables)

ii. The waveforms in the following figure are applied to the **J-K** flip – flop, and clock inputs as indicated. Determine the **Q** output, assume that the flip-flop is initially **RESET**.



(d) Design a **MOD–8** counter to count in the sequence 0,1,2,3,4,5,6 and 7 using JK Flip-Flop and logic gates. You have to show the state diagram, state table, transition table, K-map, logic expressions and the circuit implementation very clearly.

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