THE OPEN UNIVERSITY OF SRI LANKA
FACULTY OF ENGINEERING TECHNOLOGY
DIPLOMA IN TECHNOLOGY – LEVEL 3
FINAL EXAMINATION 2011/2012

00058

# MEX3272 – APPLIED ELECTRONICS

**DATE** : **29th FEBRUARY 2012**
**TIME** : **0930 HRS. – 1230 HRS.**
**DURATION** : **THREE (03) HOURS**

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**INSTRUCTIONS**

- *Question paper consists of* ***eight*** *questions. Answer* ***only five*** *questions.*
- *All questions carry equal marks.*

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***Question 01***

(a) State the Thevenin's theorem and Norton's theorem.

(b) i. Convert the following Thevenin equivalent circuit in figure Q1 (b1) to the Norton equivalent circuit.

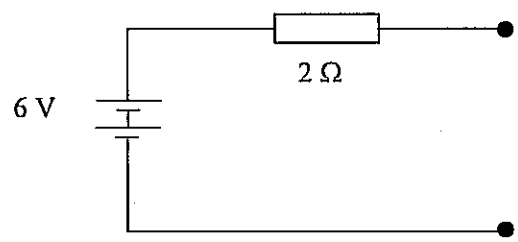



Figure Q1 (b1)

ii. Convert the following Norton equivalent circuit in figure Q1 (b2) to the Thevenin equivalent circuit.

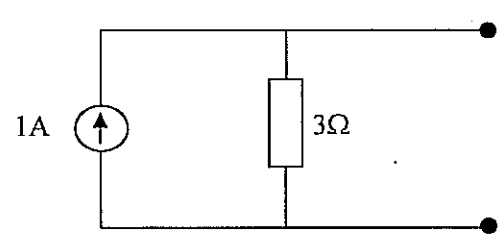



Figure Q1 (b2)

(c) Following Figure Q1(c) represents an active network consisting of two voltage sources and four linear resistors. Find the

i. Thevenin equivalent circuit,
ii. Norton equivalent circuit, across **A** and **B**.

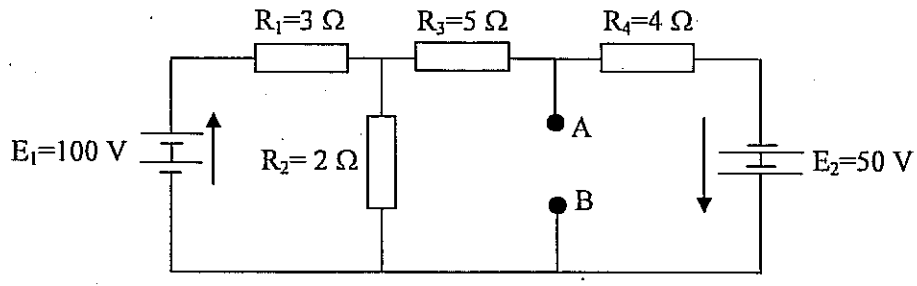



Figure Q1(c)

(d) Following Figure Q1 (d) shows a commercial Wheatstone bridge where, $V_s$ = 12V, $R_1$ = 12 kΩ, $R_2$ = 12 kΩ and $R_x$ = 6932Ω. The detector can be modeled as a 5 kΩ resistance.

i. What value of $R_3$ is required to balance the bridge?
ii. Suppose that $R_3$ is 2Ω higher than the value found in part (i). Find the current through the detector. (***Hint:*** *find the Thevenin equivalent for circuit with the detector removed. Then, place the detector across the Thevenin equivalent circuit and solve for the current*)
iii. Theoretically any value can be used for $R_1$ and $R_3$ for the bridge to balance, it is only the ratio $R_1$/ $R_3$ that is important. Explain;

1. What practical problems might occur if the values are very low?
2. What practical problems might occur if the values are very high?

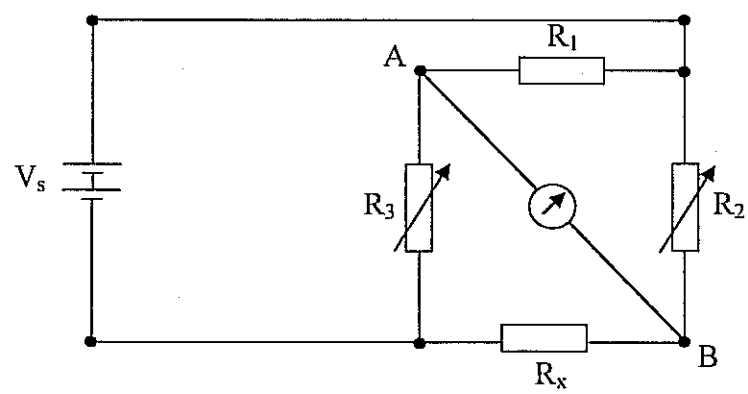



Figure Q1 (d)

***Question 02***

(a) Describe the **practical** characteristic curves of the following basic filters.
i. Low-pass ii. High-pass iii. Band-pass iv. Band-stop.

(b) Determine the center frequency ($f_c$), bandwidth (BW), quality factor (Q) and damping factor (DF) of a ***Band-pass*** filter.

(c) Describe the Butterworth, Chebyshev and Bessel filter response characteristics.

(d) Consider the circuit given in Figure Q2 (d), in which $R_1$ = 72 kΩ , $R_2$=180 kΩ , $R_3$=2.7 kΩ and $C_1 = C_2 = 0.01\mu F$.

i. Identify the filter.
ii. Determine center frequency, maximum gain and bandwidth.

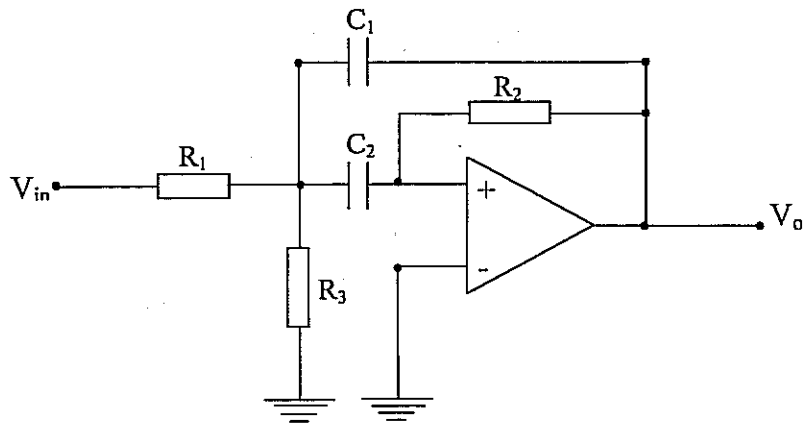



Figure Q2 (d)

***Question 03***

(a) Sketch the characteristic curve of a Diode for ***Si*** and ***Ge***.

(b) Explain the following using circuit diagrams. If the input signal is sinusoidal what is the output signal of each rectification?

i. The half wave rectification.
ii. The Bridge rectification & the Center tap rectification.

(c) Sketch the current-voltage relationship of a Zener diode in forward-biased and reverse-biased conditions.

(d)

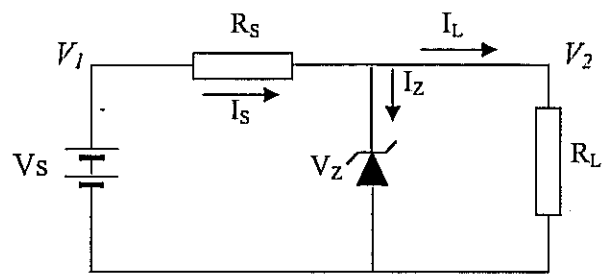



Figure Q3 (d1)

The circuit shown in Figure Q3 (d1) is a zener diode voltage regulator. Assume the zener voltage ($V_Z$) of the diode is 4.7 V and its forward bias voltage is 0.7 V.

i. What does a voltage regulator do?

ii. What would the voltage at $V_2$ be when $V_1$ = 6V if $R_L$ has the following values,

1) 1kΩ
2) 100 kΩ

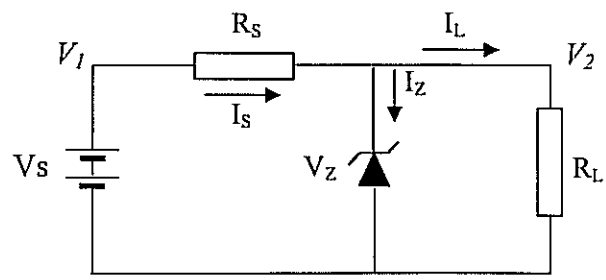



Figure Q3 (d2)

Consider the circuit shown in Figure Q3 (d2),

iii. Assuming that $V_I$ = 10V, $R_S$=1kΩ, $V_z$ = 6V, $I_{knee}$ = 1mA, find the minimum value of $R_L$, so that the diode stays in the Zener region.

iv. Assuming that $V_I$ = 10V, $R_L$ =100Ω, $V_z$ = 6V, $I_{knee}$ = 1mA, find the maximum value of $R_S$, so that the diode stays in the Zener region.

v. If $V_I$ = 10V, $R_S$ =50Ω, $R_L$ =1kΩ, $V_z$ = 6V, and the diode is in the Zener region, how much current is drawn from the source?

***Question 04***

(a) Write down the three BJT amplifier configurations for a NPN transistor.

(b) Draw the input and output characteristics of a BJT for CE configuration.

(c) Explain three biasing techniques used for a BJT with the aid of circuit diagrams.

(d) Consider the circuit shown in Figure Q4 (d1) and convert it into the circuit shown in Figure Q4 (d2) by using Thevenin's theorem and find,

(i) $R_{th}$ (ii) $V_{th}$ (iii) $I_B$ (iv) $I_C$ (v) $I_E$ (vi) $V_{CE}$

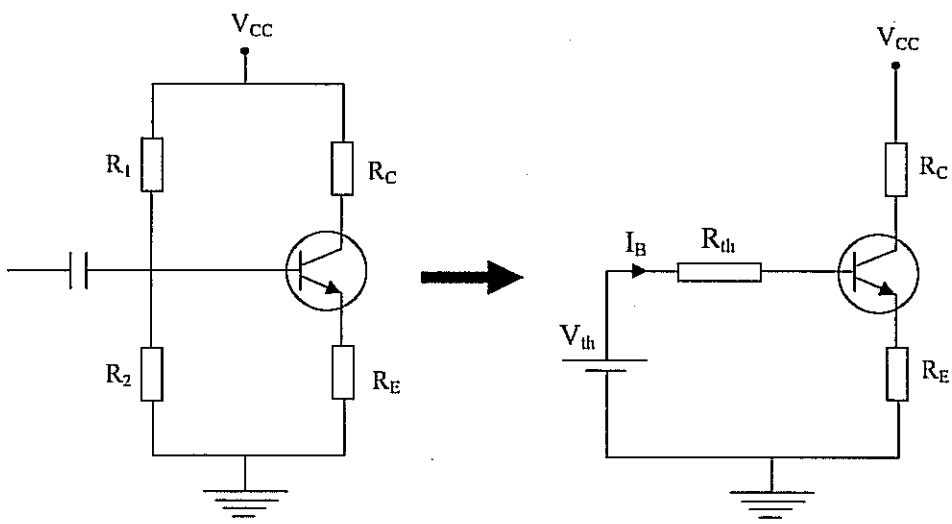



Figure Q4 (d1) Figure Q4 (d2)

**Data:** $V_{CC}$=15V, $V_{BE}$ = 0.3V, $R_1$=100 kΩ, $R_2$ = 25 kΩ, $R_C$ = 4 kΩ, $R_E$ = 6 kΩ, β = 50

***Question 05***

(a) List four properties of an ideal operational amplifier and with relevant values.

(b) Explain the following terms with regards to an operational amplifier.

i. Common Mode Rejection Ratio (**CMRR**)
ii. Output offset voltage
iii. Voltage Follower

(c)

i. What is the Slew rate of the following circuit?

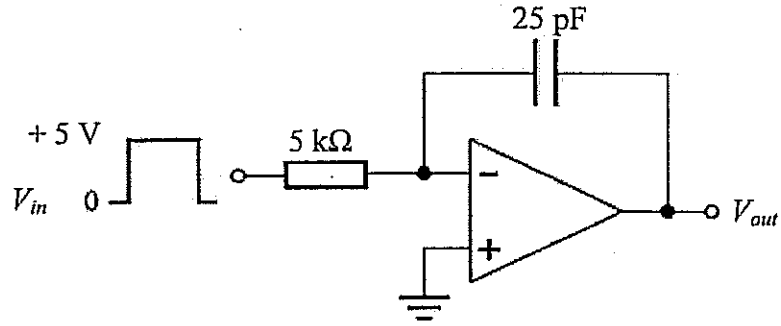



Figure Q5 (c)

ii. Design a circuit that gives ±12V using following components;
Two Op-Amps, +16V voltage source, one 4kΩ, one 12kΩ and two 15kΩ resistors.
(***Hint:*** *You may use one voltage follower and one inverting amplifier*)

(d) i. Determine an expression for the output voltage $V_{out}$ in the circuit shown in Figure Q5 (d). Assume that the operational amplifier is ideal.

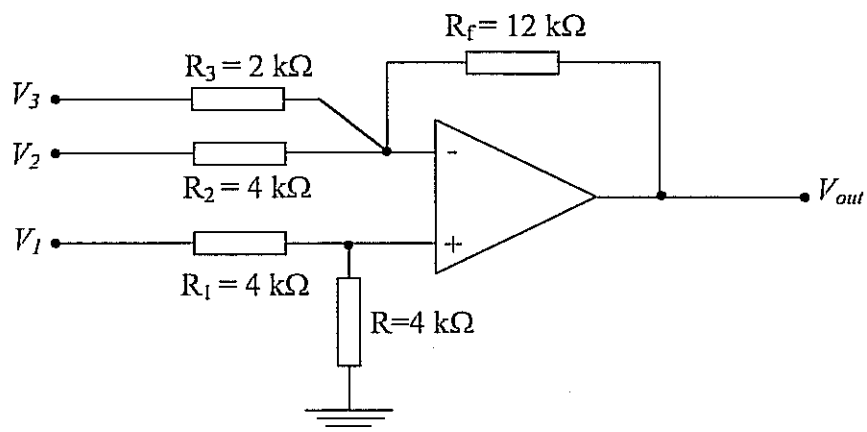



Figure Q5 (d)

ii.If $V_2$=3V and $V_3$=2V, then find the value of $V_1$ in order to get $V_{out}$ = 0 V.

***Question 06***

Explain briefly any five of the following using diagrams and mention one application for each of them.

i. Astable Multivibrator

ii. Flash Converter

iii. The Darlington Pair

iv. LDR

v. Opto coupler

vi. Successive Approximation Converter

vii. SCR

## Question 07

(a) i. Convert $101110100_2$ to Octal and Hexadecimal numbers.

ii. Express the decimal number -51 in

a. Sign magnitude method
b. 1's compliment method
c. 2's compliment method

(b) i. State De Morgan's theorem for three Boolean variables.

ii. Define the following 2-input logic elements using truth tables.

a. NAND gate
b. OR gate
c. Exclusive NOR gate

(c)

i. Given that,

$A \oplus B = A\overline{B} + \overline{A}B$

Show that

$A \oplus B \oplus AB = A + B$

ii. Implement the following Boolean function using 2-input NOR gates.

1. $f_1 = A(\overline{A} + \overline{B})(B + \overline{C}D)$

(d) i. What is half adder? Explain using truth table, Boolean expression & logic circuit.

ii. Construct full adder using two half adders & two input OR gate. Explain using truth table, Boolean expression & logic circuit.

iii. How many full adders are needed to add ***16-bit*** two binary numbers?

Take two binary numbers as follows,

1. $\mathbf{A_3\ A_2\ A_1\ A_0}$ ; Here $A_0$ is *LSB* & $A_3$ is *MSB*
2. $\mathbf{B_3 B_2\ B_1\ B_0}$ ; Here $B_0$ is *LSB* & $B_3$ is *MSB*

Summation of $\mathbf{A_0}$ & $\mathbf{B_0}$, $\mathbf{A_1}$ & $\mathbf{B_1}$, $\mathbf{A_2}$ & $\mathbf{B_2}$ ,$\mathbf{A_3}$ & $\mathbf{B_3}$ are $\mathbf{S_0}$ ,$\mathbf{S_1}$ ,$\mathbf{S_2}$ & $\mathbf{S_3}$ respectively. Consider carry out bit of summation of above two number as $\mathbf{C_{out}}$.

iv. How many full adders are needed to add ***4-bit*** two binary numbers?

v. Draw a circuit diagram to illustrate above summation using full adders.

(a) Explain briefly the meaning of the term **Combinational-logic**.

(b) i. Explain two main types of edge-triggered Flip-Flop using circuit diagrams and truth tables.

ii. Construct a D edge-triggered Flip-Flop using a JK Flip-Flop and a NOT gate.

(c) A 5-bit weighted resistor DAC consisting with minimum resistance value R has a $V_{ref} = 12V$ and a feedback resistor $R_f$.

i. Derive an expression for $V_{out}$.
ii. If $R_f = R$, find the resolution and the full scale analog output voltage.
iii. Find the $V_{out}$ when the input is 101011.

(d) Design a synchronous counter with the irregular binary count sequence 1,2,3,5 and 7 using JK Flip-Flops and logic gates (if required). You have to show the state diagram, state table, transition table, K-map, logic expressions and the circuit implementation very clearly.

**-END-**