# The Open University of Sri Lanka
# Faculty of Engineering Technology

| | | |
|---|---|---|
| Study Programme | : | Diploma in Technology/Bachelor of Technology (Engineering) |
| Name of the Examination | : | Final Examination |
| **Course Code and Title** | : | **MEX3272 – Applied electronics** |
| Academic Year | : | 2012/13 |
| Date | : | 31st July 2013 |
| Time | : | 0930Hrs.-1230Hrs. |
| Duration | : | 3 hours |

**General instructions**

1. Read all instructions carefully before answering the questions.
2. This question paper has eight questions.
3. Answer five questions only.

---

***Question 01***

(a) Describe Nodal and Mesh analysis.

(b) i. Write the equations needed to solve for the mesh currents in figure Q1 (b).

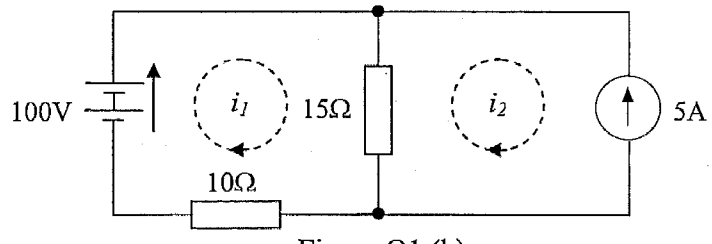



Figure Q1 (b)

(c) Thevenin's equivalent circuit shown in figure Q1(c). $R_L$ is variable resistor. Find,

i. the power ($P_L$) delivered to the load $R_L$.
ii. the relationship between $R_{th}$ and $R_L$ for maximum power dissipation ($P_{Lmax}$) in the circuit.
iii. the maximum power dissipation in the circuit only with $R_{th}$ and $V_{th}$.

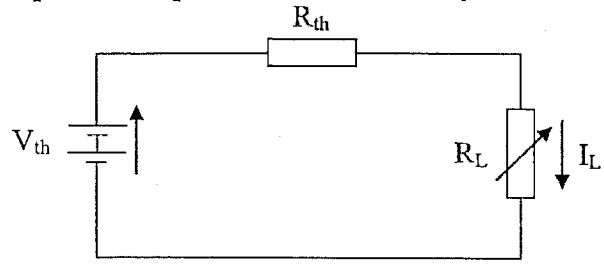



Figure Q1 (c)

(d) Following figure Q1 (d) represents an active network consisting of two voltage sources, one current source and four linear resistors. Find the current $I_L$ through $R_L$ using Thevenin's theorem.

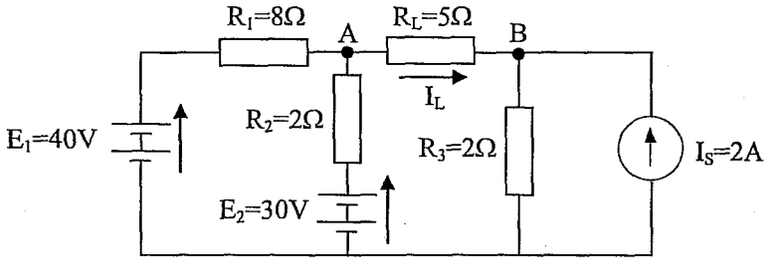



Figure Q1 (d)

***Question 02***

(a) List four basic categories of active filters.

(b) Describe followings for above mentioned filters.

i. Characteristics curve of practical and ideal case.
ii. Center frequency ($f_o$) of the filter.

(c) Consider the circuit given in the figure Q2 (c).

i. Identify the filter order and the type.
ii. Determine the transfer function of the filter.
iii. Find the pass band gain of the filter.

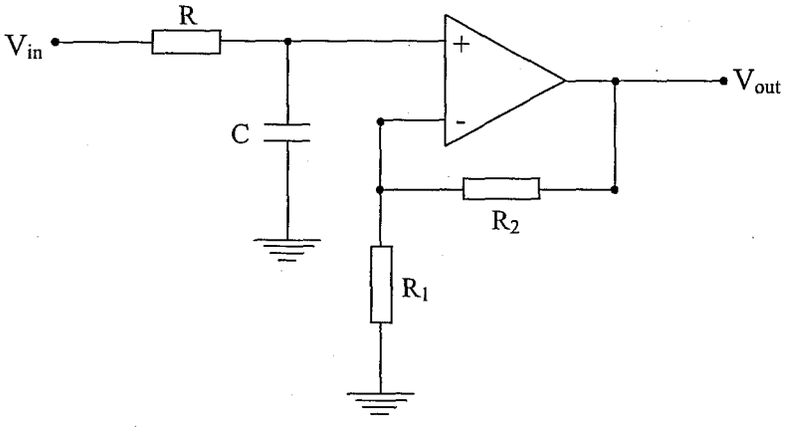



Figure Q2 (c)

(d) Design a first order low-pass filter with a cut-off frequency at 1 kHz and pass band gain of two (02). Draw the frequency response of the circuit.

***Question 03***

(a) i. Sketch the forward and reverse characteristic curve of a Diode.

ii. The sinusoidal voltage (20V) is applied to the biased parallel clipper circuit of figure Q3 (a). Find the wave shape of the output voltage $V_o$. Assume that two diodes are ideal.

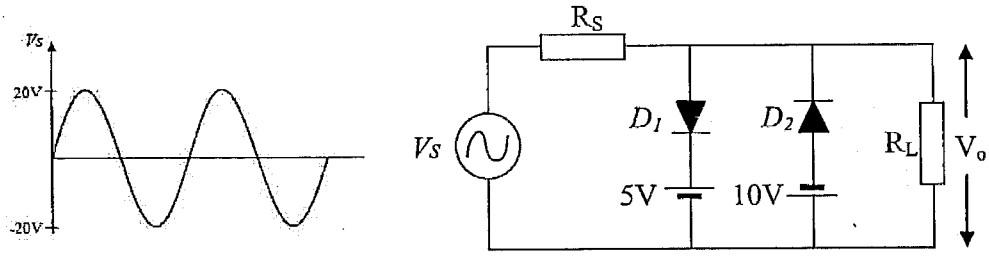



Figure Q3 (a)

(b) i. Sketch the V- I characteristics of a Zener diode.

ii. The sinusoidal voltage (20V) is applied to the circuit shown in figure Q3 (b). Find the wave shape of the output voltage $V_o$.

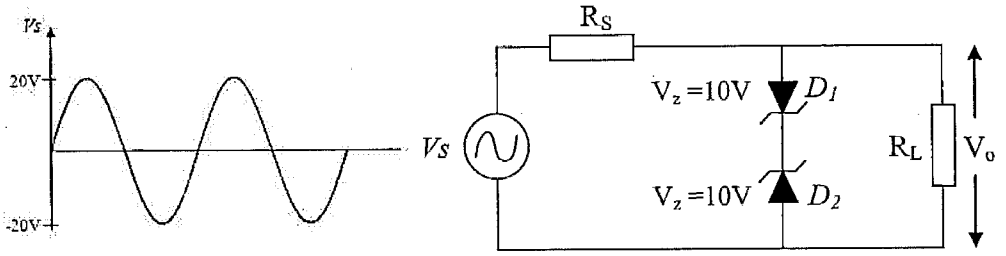



Figure Q3 (b)

(c) The load resistance $R_L$ in the voltage regulator circuit of figure Q3 (c) is fixed at 12kΩ. But the input supply voltage $V_S$ varies from 90V to 120V.

i. When the input supply voltage reduces to 90V, does Zener remain "ON"?
ii. Calculate the maximum Zener diode current $I_{Z\,(max)}$.
iii. Calculate the minimum Zener diode current $I_{Z\,(min)}$.

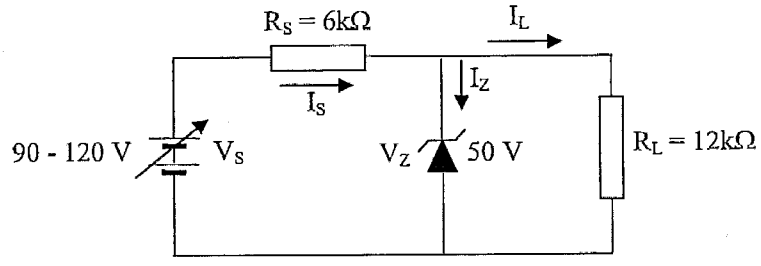



Figure Q3 (c)

*Question 04*

(a) We use semiconductors to build Bipolar Junction Transistor (BJT). Show how those different types of semiconductors are connected to form BJT. Give the circuit symbol of different type of the BJT.

(b) Show the different regions of operation of a BJT on its collector characteristics.

(c) i. In a good biasing circuit, the operating point should not shift if the temperature varies or the transistor parameters change. List three biasing techniques used for a BJT to have a good bias circuit.

ii. The transistor in the fixed bias circuit of figure Q4 (c) has a dc current gain of 50. If, $V_{CC} = 12V$, $R_B = 300\ k\Omega$, $R_C = 2\ k\Omega$. Determine its Q-point.

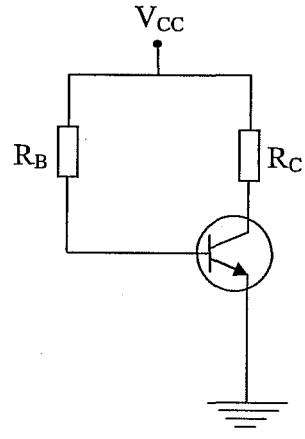



Figure Q4 (c)

(d) A common emitter transistor amplifier circuit is shown in figure Q4 (d). The transistor is made using silicon semiconductors.

i. Calculate the quiescent voltages and currents by using Thevenin's theorem.
ii. Find the small signal mid band voltage gain of the circuit.
Where; $V_{CC} = 12V$, $R_1 = 18k\Omega$, $R_2 = 3.3k\Omega$, $R_C = 1.5k\Omega$, $R_E = 270\Omega$, $\beta = 100$

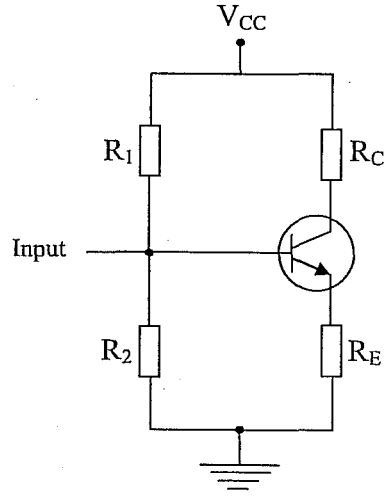



Figure Q4 (d)

***Question 05***

(a) List five properties of an ideal Operational Amplifier and compare those with practical Operational Amplifier.

(b) Explain following terms of an Operational Amplifier.

i. Input offset current
ii. Slew rate
iii. Common Mode Rejection Ratio (**CMRR**)

(c) Following circuit in figure Q5 (c) designed to get ±15V when we have 20V ($V_{cc}$) voltage source.

i. Identify ***Circuit A*** & ***Circuit B***.
ii. Find the suitable values for $R_1$, $R_2$, $R_3$ and $R_f$ to get ±15V
iii. Calculate the value of $V_x$, $V_{out1}$ and $V_{out2}$

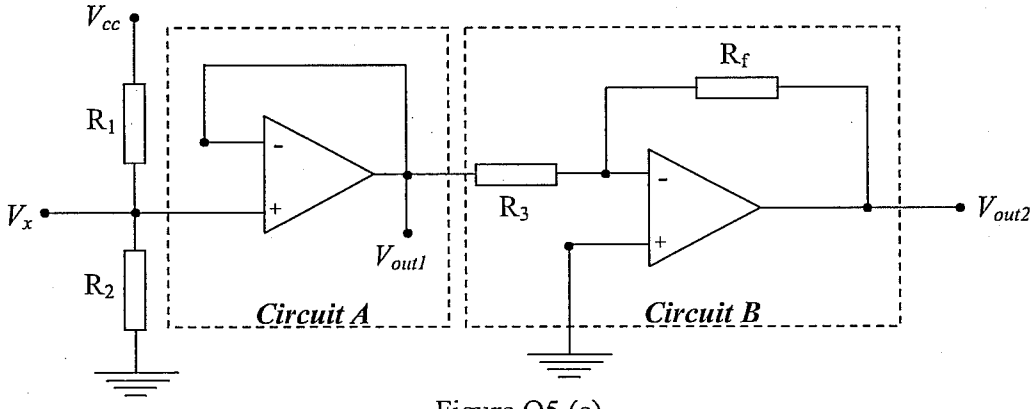



Figure Q5 (c)

(d) Assume that the Operational Amplifier of figure Q5 (d) is ideal. Determine the value of **R** when $V_{out} = V_1 + V_2 - V_3 - V_4$.

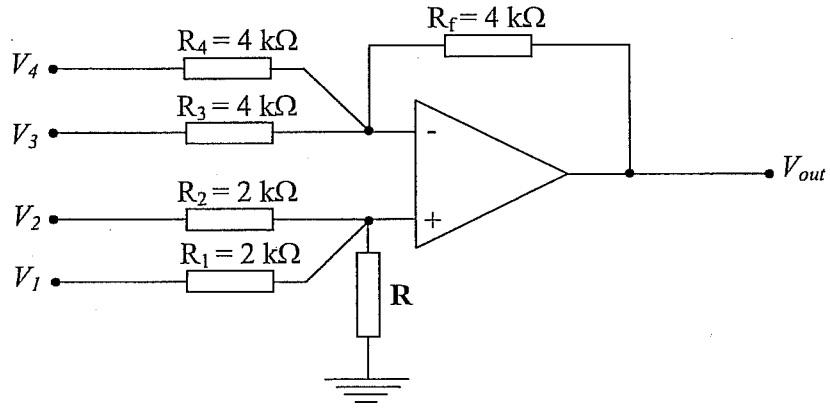



Figure Q5 (d)

***Question 06***

Explain briefly any five of the following using diagrams and describe one application for each of them.

i. Flash Converter
ii. The Darlington Pair
iii. LDR
iv. Opto coupler
v. Sample and Hold Circuit
vi. SCR
vii. The Push Pull Power Amplifier

***Question 07***

(a) i. Convert $101010010_2$ to Octal number.

ii. Convert $101001111_2$ to Hexadecimal number.

iii. Express the decimal number -63 in Sign magnitude method.

iv. $11100110_2$ is representing by 1's compliment method. What is the decimal value?

v. $11100001_2$ is representing by 2's compliment method. What is the decimal value?

(b) i. State De Morgan's theorem for four Boolean variables A, B, C and D.

ii. Define the following 2-input logic elements using Boolean function and truth tables.

a. NOR gate
b. Exclusive OR gate

(c) i. Implement the NOT, AND and OR gates logic function for two variables A and B by using only NOR gate(s).

ii. Implement the following Boolean function using 2-input NOR gates.

$$f = (A \bullet B) + (C \bullet \overline{D})$$

iii. Simplify the following function using Karnaugh map.

$$f(A,B,C,D) = \Sigma(0,1,2,3,4,8,9,10,12,13)$$

(d) There is a combinational logic circuit which is having four input bits as **A, B, C and D** where **A** and **D** are the most and least significant bits respectively. The output of the circuit (*f*) is "**TRUE**" or "**1**" if the input is divisible by 3, 5 or greater than or equal 13 otherwise the output is **"FALSE"** or **"0"**. Assume that **ZERO** is not divisible by any number.

i. Construct the truth table for above logic.

ii. Write the Boolean expression for the output (*f*) and simplify it using Karnaugh map.

iii. Design a circuit using logic gates (OR, AND and NOT) to carry out the function.

***Question 08***

(a) What is the different between **Combinational-logic** and **Sequential-logic**?

(b) i. Briefly describes the **JK** edge-triggered flip-flop and the **SR** edge-triggered flip-flop using circuit diagrams and truth tables.

ii. Construct a **D** edge-triggered flip-flop using a SR flip-flop and a NOT gate.

(c) The waveforms in the following figure Q8 (c) are applied to the **SR** flip - flop, and clock inputs as indicated. Determine the **Q** output, assume that the ***positive edge-triggered*** flip-flop is initially **RESET**.

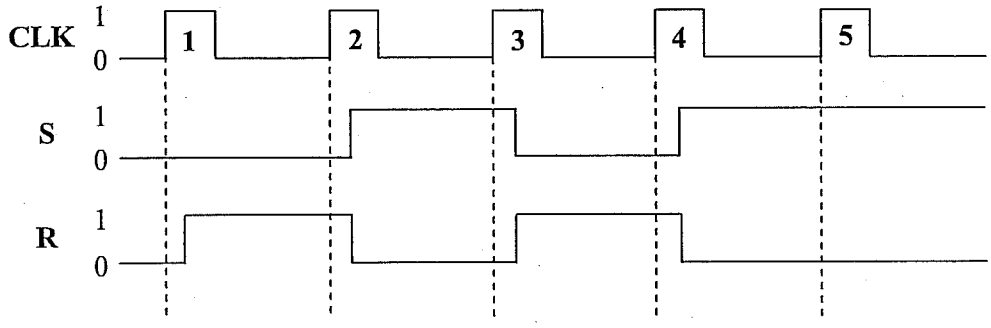



Figure Q8 (c)

(d) Design a synchronous counter with the irregular binary count sequence 1,2,4,6 and 7 using JK Flip-Flops and logic gates (if required). You have to show,

i. The state diagram
ii. The state table
iii. The transition table for JK
iv. The K-map
v. The logic expressions
vi. The circuit implementation, very clearly.

**-END-**