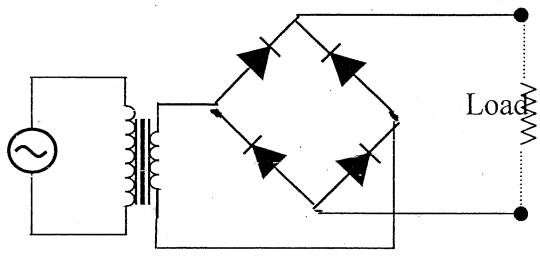
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The Open University of Sri Lanka
B.Sc./B.Ed Degree Programme Level-03/5
Final Examination - 2015/2016
PCU 1170/ PCU 3170 - Electronics for Biology Students
Duration : Two (2) hours

Date: 3rd July 2016 **Time: 1.00 p.m.- 3.00 p.m**

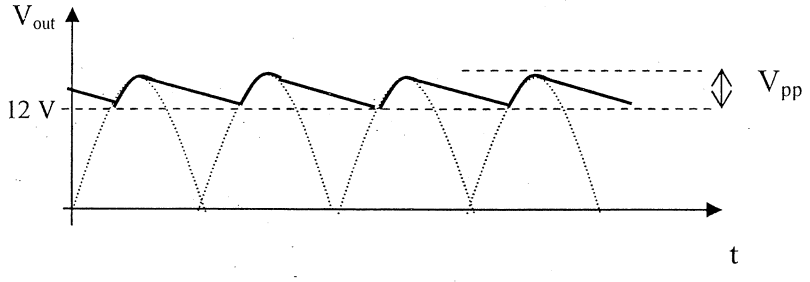
Answer four (4) questions only

1. Most of the regular electronic devises are operated at low dc voltages. The following circuit diagram shows the first steps of a low dc voltage power supply connected with a load.



(i) Briefly explain the function of each step of the above circuit with the help of a sinusoidal voltage signal.

(ii) How do you connect a 100 μF electrolytic capacitor with the above circuit to obtain the following voltage pattern (dark lines) across the load?

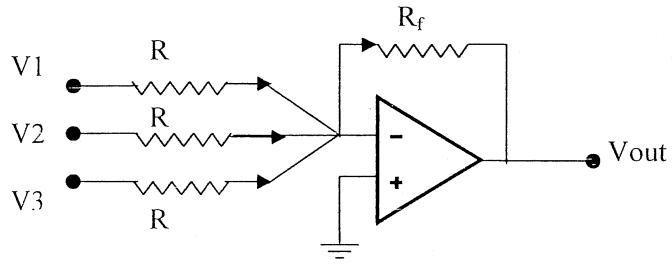


(iii) Derive an approximate equation for the ripple voltage (V_{pp}) of the above voltage pattern and then calculate the value of V_{pp} when the current (I) through the load is 2000 mA and the frequency of the input voltage signal to the transformer is 50 Hz.

(iv) If the lowest voltage of the above pattern is 12 V, how do you modify the above circuit to obtain a stabilized 5 V dc voltage ?

(v) In addition to the positive and negative polarities, a cell phone battery consists of two extra terminals. What is the function of these two extra terminals when the battery is being charged?

2. (i) Name the terminals of a general purpose Op-amp IC.
   (ii) Define the open loop voltage gain.
   (iii) (a) The circuit diagram of a summing amplifier shown below is used to add three voltages.



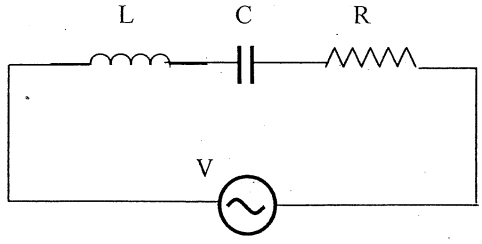
Using the golden rules , derive the equation for the output voltage (V_{out}).

(b) Modify the above circuit by adding another stage of an Op-amp to obtain the final result as ; $V_{out} = V_1 + V_2 + V_3$.

(iv) (a) What are the ideal impedance at the input and output of an Op-amp ?

(b) Use an Op-amp , to link an audio amplifier having high output impedance and a speaker having low input impedance to match the impedance.

3. The following figure shows an alternative current circuit consisting of ac voltage source (V) , an inductor (L), a capacitor (C) and a resistor (R).



(i) If the angular frequency of the voltage signal is ω , derive an equation for the total impedance of the circuit .

(ii) The values of components are as L = 50 mH , C = 1 μF , R = 1 kΩ and $\omega = 2 \times 10^4$ rads^{-1}. Calculate the total impedance of the circuit.

(iii) The peak voltage across the resistor is 1.5 V. Find the peak current through the circuit.

(iv) Hence find the peak voltages across the other components (L and C).

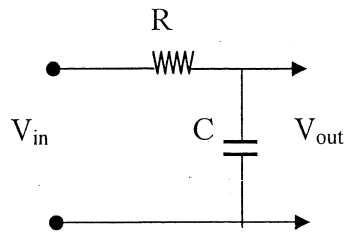
(v) Draw the voltage pattern across L and C compared to R on the same time axis.

(vi) At which angular frequency , this circuit gains maximum current ?

4. (i) (a) The ratings of an LED is 2.6 V/ 30 mA. How do you connect this LED with a 9 V battery ?
(b) Calculate the light energy released by the LED during 2 minutes.

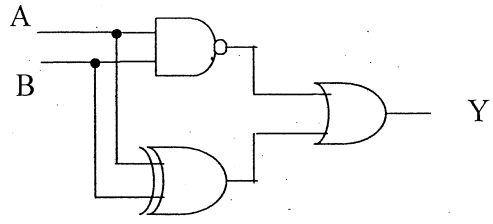
(ii) (a) Draw the circuit diagram of positive- peak-clipping circuit using resistors and a rectifier diode.
(b) Obtain the wave pattern at the output of this circuit for a sinusoidal input voltage signal. Give brief explanation for your pattern.

(iii) (a) The following circuit can be used as a simple low pass filter .



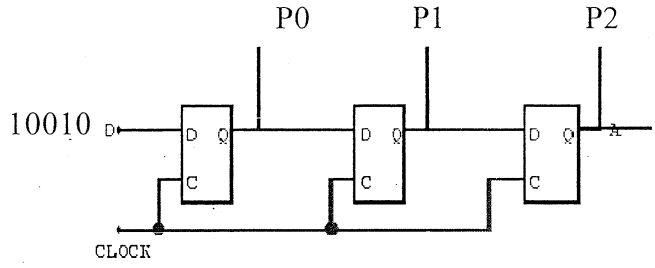
Explain its function considering two sinusoidal signals which are at low and high frequencies.
(b) Sketch a graph for the voltage gain of this circuit against the frequency.

5. (i) Give the truth tables for OR gate , Ex-OR gate & NAND gate.
(ii) (a)Derive the Boolean expression for the following logic circuit.



(b) Give the truth table for the above circuit for all the possible logic levels (0 or 1) at A and B inputs.
(iii) (a) Write down De Morgan's theorem used in Boolean algebra.
(b) Using the De Morgan's theorem show that OR gate can be constructed using NAND gates.
(c) Use Morgan's theorems to simplify ; $F = \overline{(A.\bar{B}).(\bar{B}+C)}$.

6. (i) Draw any sequential logic circuit using simple logic gates.
   (ii) Draw the symbol of a R-S Flip-flop and give the truth table.
   (iii) Modify a R-S Flip-flop as a D- Type Flip – flop and give the truth table for it.
   (iv) The following diagram shows a three bit shift register constructed with D-type Flip-flops.



A binary number ; 10010 is fed to the system applying clock pulses. Give the binary state at the outputs (P0, P1 and P2) after three clock pulses.

(v) Draw a three-bit ripple counter circuit using J-K Flip-flops and draw the timing diagrams at each output for five consecutive clock pulses.

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