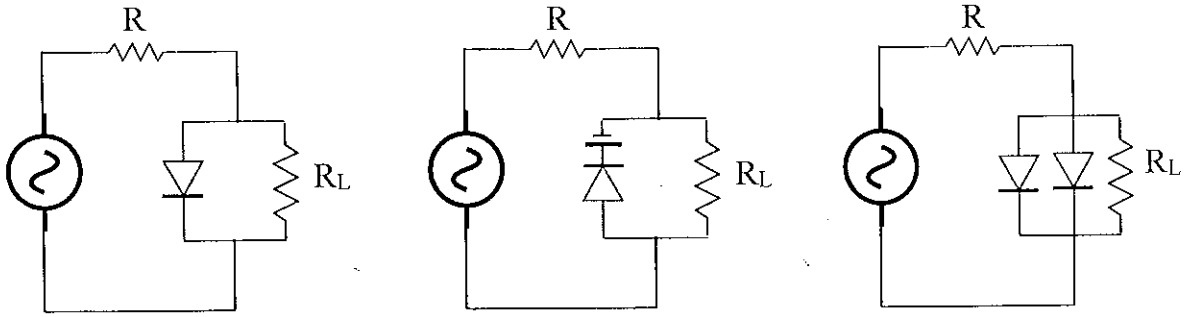
The Open University of Sri Lanka
B.Sc./ B.Ed Degree Programme Level 05
Final examination - 2017/2018
PHU5318 / PCU 3170 – Electronics for Biology Students
Duration : Two (2) Hours

Date: 25th September 2018 **Time : 9.30 am - 11.30 am**

Answer only four (4) questions

(1) (i) A sinusoidal voltage signal is connected to the following circuits which consist of diodes resistors and dc batteries. The output is taken across R_L.



(a) (b) (c)

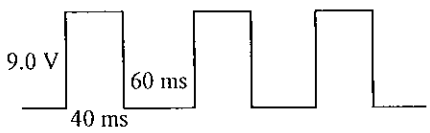
Sketch the input and output voltage signals on the same time axis.

(ii) A square pulse is connected with the following pulse shaping circuits and the output is received across AB. Sketch the input and output voltage patterns on the same time axis.



(a) (b)

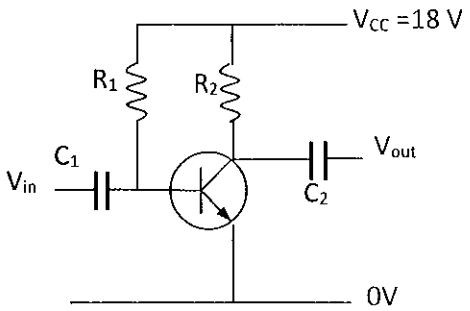
(iii) A square voltage signal shown in the following figure is connected in series with a resistor (R) and an LED (2.3V/ 35 mA).



(a)Calculate the value of the resistor

(b) Calculate the power dissipated through the resistor during a 1 s time period.

(2) Following single-stage transistor circuit can be used to amplify an alternative voltage signal.



a) The transistor given in the circuit is forward biased with 0.7 V. What would be the value of R_1, if the current through it is 35 mA ?

b) If the current gain (β) of the transistor is 150 , find the value of R_2 to maintain the voltage at the collector as half of the supply voltage (V_{cc})

c) Under the above condition, a sinusoidal voltage signal, which is connected at V_{in} produces a base current with an amplitude of 2 mA. Calculate maximum voltage at the output.

d) Draw the output wave pattern comparing the input.

(3) (a) Three electrical components; R = 100 Ω, C = 1 μF and L = 75 mH are connected in series with a 2.3 kHz voltage signal. Draw the circuit diagram.

(b) Write down the impedance of each component and then find the total impedance.

(c) If the peak voltage across the capacitor is 150 mV. Find the peak current through the circuit

(d) Find the peak voltages across the other two components in the circuit.

(e) Derive a general equation for the resonance frequency of the above circuit and then calculate the resonance frequency of the circuit.

(4) (a) Draw the circuit diagram to construct a 9 V/ DC power supply starting from 230 V /50 Hz main power supply (do not use any ICs).

(b) The following diagram shows the voltage pattern produced at the output from a circuit;



Write down an equation for the peak to peak voltage (V_{pp}) of the ripple signal when the value of the connected capacitor is C, frequency of the input voltage signal is f and assuming the constant discharging current through the capacitor as I.

(c) Calculate the minimum value of the capacitor to maintain the peak to peak voltage of the ripple signal bellow 2 V, when the discharging current is 20 mA.

(d) Write down two disadvantages of above circuit, when the load resistance at the output changes.

(e) Draw an additional circuit diagram for the above circuit to construct a voltage variable power supply using the IC named; LM 317.

(5) (a) Define the differential voltage gain (open loop voltage gain ; A_d) of an operational amplifier.

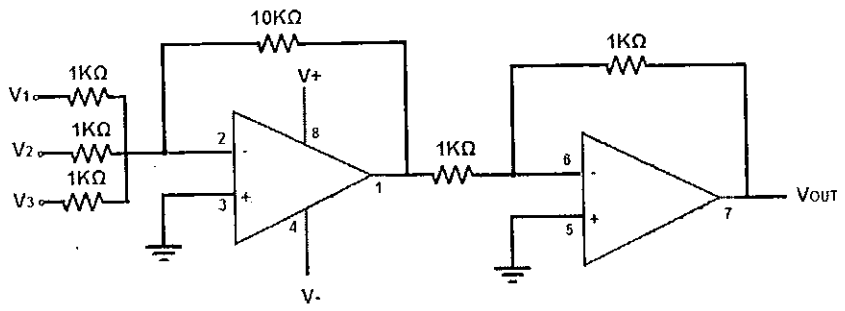
(b) Why does the output voltage of an open loop amplifier saturate even at a very low voltage difference at the input? For this situation, sketch a graph for the output voltage against the input voltage difference.

(c) Write down the two golden rules for a closed loop operational amplifier.

(d) Derive the equation for the voltage gain of an inverting amplifier; $\frac{V_{out}}{V_{in}} = -\frac{R_f}{R_{in}}$

where, R_{in} and R_f are the values of resistors used at the input and feedback paths, respectively.

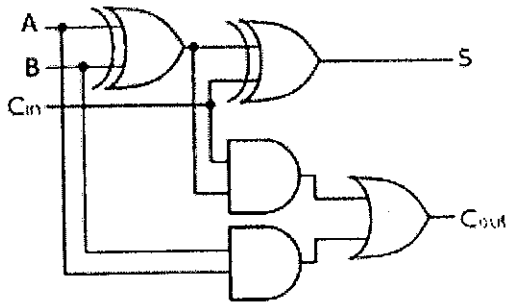
(e) Find the output voltage of the first summing amplifier (terminal No: 1) given in the following circuit by considering the inputs as V_1 ,V_2 and V_3



(f) Calculate the output voltage of each operational amplifier (terminal No: 1 and 7) when $V_1 = 2$ mV, $V_2 = 1$ mV and $V_3 = 5$ mV.

(6) (i) Give the truth tables for AND , OR and Ex-OR gates .

(a) Derive the expression for the following combinational logic circuit and give the truth table, considering A, B & C_{in} as the inputs and S & C_{out} as the outputs.



(b) Taking any combination of A, B and C_{in} (at the same time all are not zero) show that the above circuit behaves as a full adder circuit.

(c) Two binary numbers N_1= 1101 and N_2 = 1110 are added using the above circuit and first few steps are given in the following table. Redraw the table in your answer script and complete the table to get the final answer.

	2^3	2^2	2^1	2^0
N_1	1	1	0	1
N_2	1	1	1	1
C_{in}				
S				0
C_{out}				1

(ii) (a) What is the advantage of the clock input in a clocked JK flip-flop ?

(b) Draw a circuit diagram of a four bit binary clock using negative edge triggered JK flip-flops.

(c) Explain how the 1st bit (2^0) and 2nd bit (2^1) at the output changes with the next clock pulse applied to the first JK flip-flop when the output appears as follows.

2^0 2^1 2^2 2^3

1 0 1 1

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