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THE OPEN UNIVERSITY OF SRI LANKA
FACULTY OF ENGINEERING TECHNOLOGY
LEVEL 3
FINAL EXAMINATION 2010/2011

MEX3272 – APPLIED ELECTRONICS

LIBRARY
01 NOV 2011

DATE : **09th MARCH 2011**
TIME : **0930 HRS. – 1230 HRS.**
DURATION : **THREE (03) HOURS**

INSTRUCTIONS

- *Question paper consists of **eight** questions. Answer **only five** questions.*
- *All questions carry equal marks.*

Question 01

(a) State the Thevenin's theorem and Norton's theorem.

(b) DC circuit is shown in Figure Q1 (b1).Use source transformation to find the values of **A** (Voltage source), **B**, **C**, **D** (Resistors), $\mathbf{I_x}$ (Current through the circuit) as shown in Figure Q1 (b2).

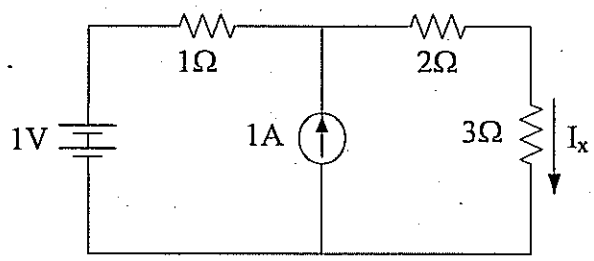


Figure Q1 (b1)

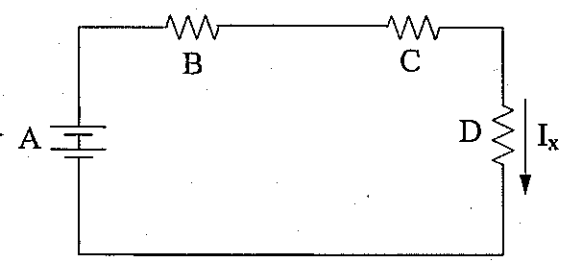


Figure Q1 (b2)

(c) Find R_{load} for maximum power dissipation in the circuit shown in Figure Q1 (c).

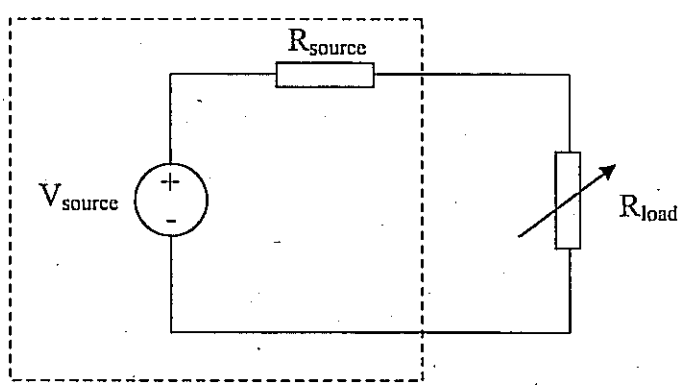


Figure Q1 (c)

(d) Figure Q1 (d) represents an active network consisting of three voltage sources and six linear resistors. Find the,

i. Thevenin equivalent circuit,
ii. Norton equivalent circuit, at the terminals **A** and **B**.
iii. Calculate the power dissipated in a 3Ω resistor connected between the terminals **AB**.

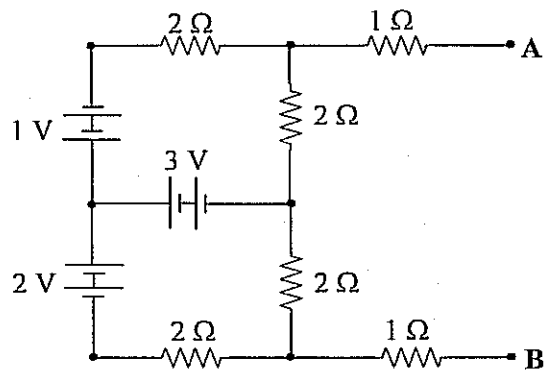


Figure Q1 (d)

Question 02

(a) Compare the **practical** and **ideal** characteristic curves of the basic filters as low-pass, high-pass, band-pass and band-stop.

(b) Give an expression for the center frequency (f_c), bandwidth (BW), quality factor (Q) and damping factor (DF) of a band-pass filter.

(c) Explain the Butterworth, Chebyshev and Bessel filter response characteristics.

(d) Consider the circuit given in Figure Q2 (d). Determine,

i. The center frequency (f_c)
ii. Quality factor (Q)
iii. Bandwidth (BW), for the band pass output of the state variable filter.

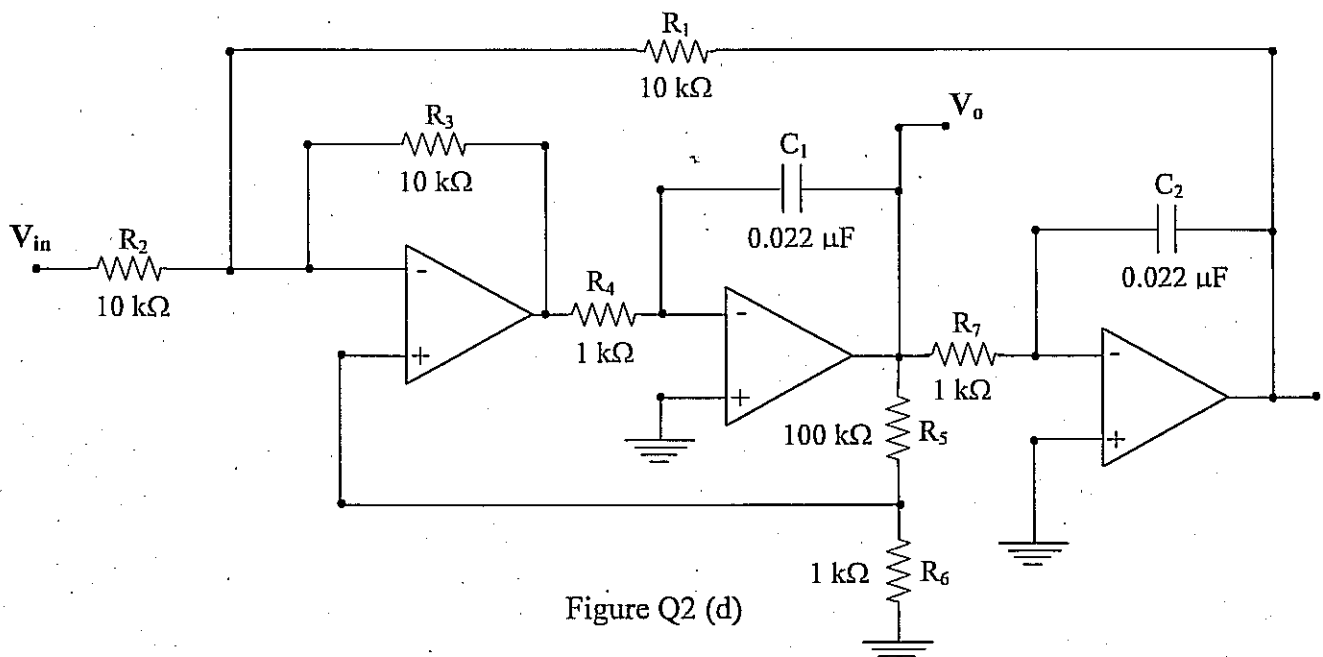


Figure Q2 (d)

Question 03

(a) Give five types of diodes. Sketch the characteristic curve of a silicon Diode.

(b) Explain the following rectification methods using circuit diagrams, and show the output for a sinusoidal input.

i. Half wave rectification
ii. Full wave rectifications (Centre tap and Bridge rectification).

(c) Sketch the I_D Vs V_D for a zener diode showing the various regions of operation.

(d) A voltage regulator circuit is shown in Figure Q3 (d). Calculate the values of V_o, I_L, I_S and I_C. Assume that the transistor is ***Silicon***.

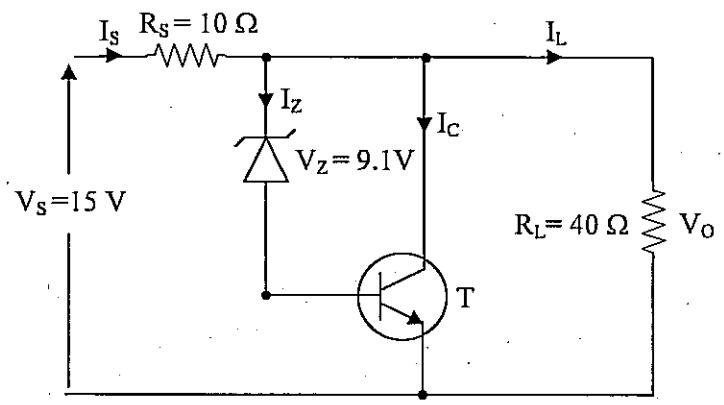


Figure Q3 (d)

Question 04

(a) Write down the three bipolar transistor configurations for a NPN transistor.

(b) Draw the input (I_B Vs V_{BE}) and output (I_C Vs V_{CE}) characteristics of a bipolar transistor.

(c) Explain three biasing techniques used for a bipolar transistor with the circuit diagrams.

(d) Consider the common emitter transistor amplifier circuit as shown in Figure Q4 (d). The transistor is silicon.

i. Calculate the quiescent voltages and currents. Use Thevenin equivalent circuit.
ii. Find the small signal mid-band voltage gain of the circuit.

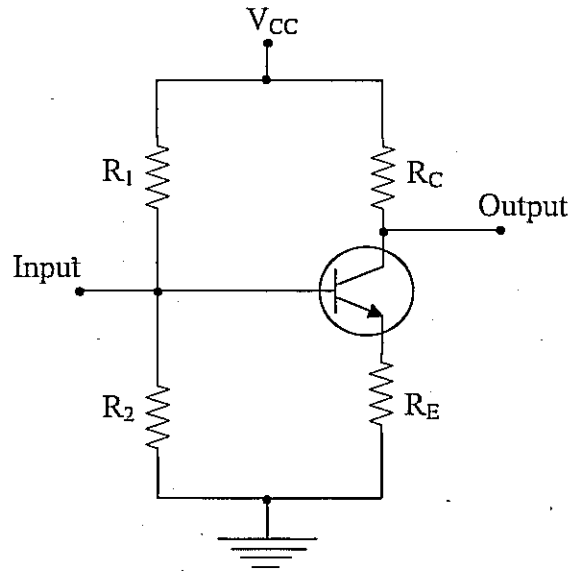


Figure Q4 (d)

Where: V_{CC}=12V, V_{BE} = 0.6V, R_1=18kΩ, R_2 = 3.3kΩ, R_C = 1.5kΩ, R_E = 270Ω, β = 100

Question 05

(a) Give five characteristics of an ideal operational amplifier (Op-Amp) and compare the ideal values with its typical values.

(b) Explain the following terms with regards to an operational amplifier

i. Output offset voltage
ii. Input bias current
iii. Common Mode Rejection Ratio (**CMRR**)

(c)

i. Explain the voltage follower using a circuit diagram and find the voltage gain of it?

ii. Determine an expression for the output voltage V_{out} in the circuit shown in Figure Q5 (c). Assume that the operational amplifier is ideal

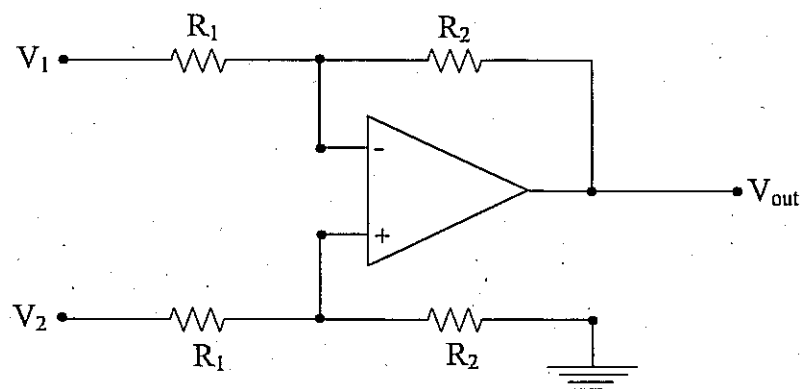


Figure Q5 (c)

(d) The circuit shown in Figure Q5 (d) uses a resistive transducer (R_D). According to the temperature it varies by ΔR.

i. Determine an expression for V_{XY}
ii. If $R_T = R_A = R_B = R_C = R$ then prove that $\mathbf{V_{XY} = [(- V_{in})(\Delta R)]/(4R)}$
iii. Find an expression for V_{in}

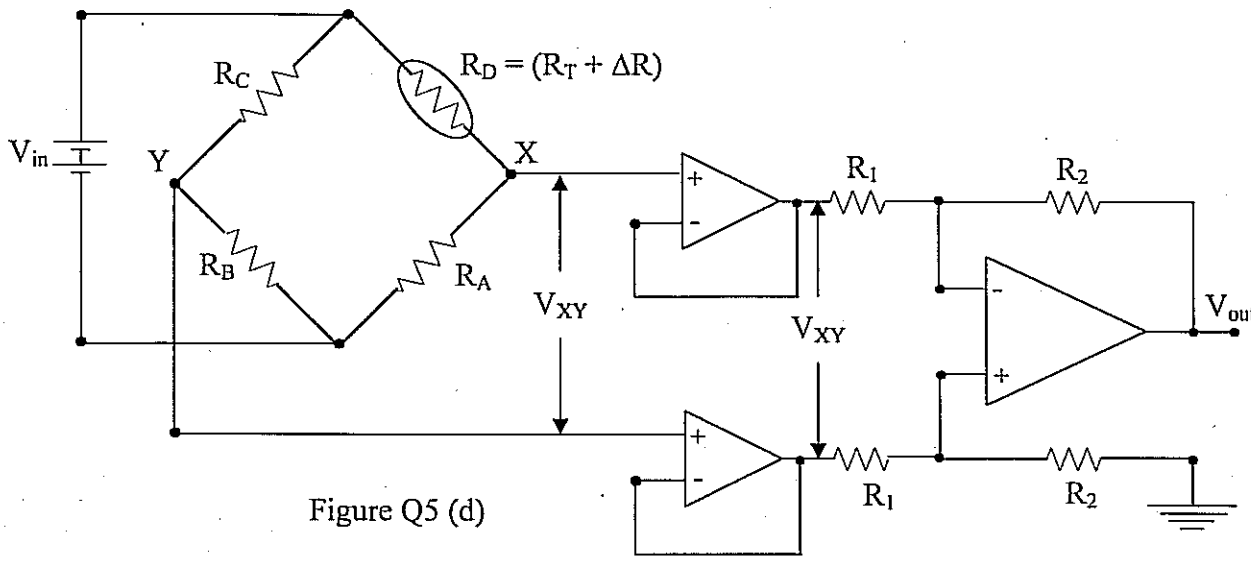


Figure Q5 (d)

Question 06

Explain briefly any five of the following using diagrams and mention one application for each of them.

i. Flash Converter
ii. The Push Pull Power Amplifier
iii. Astable Multivibrator
iv. Opto coupler
v. The Darlington Pair
vi. Successive Approximation Converter
vii. SCR

Question 07

(a) i. Convert 1100101001010111_2 to Octal and Hexadecimal numbers.

ii. Express the decimal number -34 in
   a. Sign magnitude method
   b. 1's compliment method
   c. 2's compliment method

(b) i. State De Morgan's theorem for three Boolean variables A, B and C.

ii. Define the following 2-input logic elements using truth tables.

a. NOR gate
b. NAND gate
c. Exclusive OR gate

iii. Realize the following logic function using 2-input NOR gates.

$$f_1 = A.B + \overline{A}B$$

(c) i. Prove that following identity,

$$(A \oplus B \oplus AB)(A \oplus C \oplus AC) = A + BC$$

ii. Simplify the following function using Karnaugh map.

$$f(A,B,C,D) = \sum(0,1,2,3,4,9,10,13,14)$$

(d) The input to a combinational logic circuit is a 4-bit binary number **ABCD** where **A** and **D** are the most and least significant bits respectively. The output of the circuit is **"TRUE"** or **"1"** if the input is divisible by 4 or greater than 10 otherwise the output is **"FALSE" or "0"**. Assume that zero is not divisible by any number.

i. Write the Boolean expression for the output (*f*) and simplify it using Karnaugh map, Show the steps very clearly.
ii. Design a circuit using logic gates (OR, AND and NOT) to carry out the function.

Question 08

(a) Explain briefly the different between **"Combinational-logic"** and **"Sequential-logic"**.

(b)

i. Briefly describe the difference between JK edge-triggered flip-flop and SR edge-triggered flip-flop using circuit diagrams and truth tables.

ii. Construct a D edge-triggered Flip-Flop using a SR Flip-Flop and a NOT gate.

(c) i. Explain basic data movement in shift registers. (Use four bits to illustrate).

ii. Explain 4-bit ***Johnson ring counter*** (Show a circuit diagram using D flip-flops and the sequence of ring counter).

(d) Design a synchronous counter with the binary count sequence 1,3,4,6 and 7 using JK Flip-Flops and logic gates. You have to show the state diagram, transition table, K-map, logic expressions and the circuit implementation very clearly.

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