The Open University of Sri Lanka
Faculty of Engineering Technology

Study Programme	:	Diploma in Technology/Bachelor of Technology (Engineering)
Name of the Examination	:	Final Examination
Course Code and Title	:	**MEX3272 – Applied electronics**
Academic Year	:	2013/14
Date	:	13th August 2014
Time	:	0930hr-1230hr
Duration	:	3 hours

General instructions

1. Read all instructions carefully before answering the questions.
2. This question paper has **eight** questions.
3. Answer **five** questions only.

Q1

(a) Draw circuit symbols of a diode and a zener diode. Sketch their V/I characteristics.

[4 marks]

(b) What are the full wave rectification methods? Explain them using circuit diagrams. Draw the output wave form if input is a sinusoidal signal.

[6 marks]

(c) Figure Q1 shows the emitter follower regulation circuit. Calculate the values of V_L , I_L , V_{CE} and power dissipated by T_1.Assume that the transistor is made out of silicon.

[10 marks]

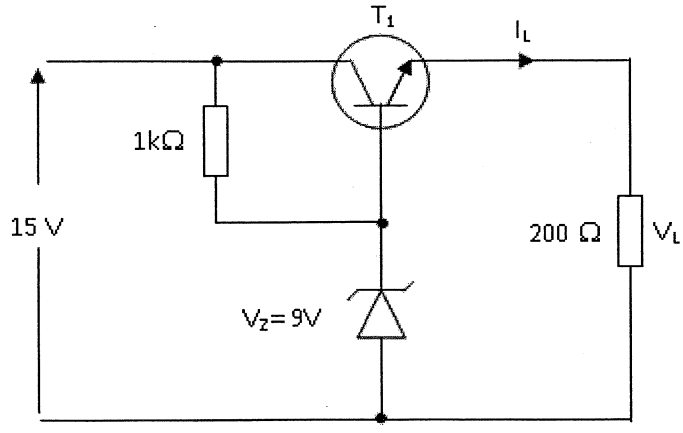


Figure Q1

Q2

A linear potentiometer is used to measure fractional linear distance x. The potentiometer track has resistance R_P connected to a voltage V_S.

(a) Show that with a load of resistance R_L the output voltage V_L across the load as a proportion of the supply voltage V_S is given by:

$$\frac{V_L}{V_S} = \frac{xR_LR_P/(R_L + xR_P)}{R_P(1-x) + xR_LR_P/(R_L + xR_P)}$$

[10 marks]

(b) Show that if R_L is infinite (an open circuit) the output voltage V_L is proportional to distance x. [4 marks]

(c) Show that with a finite value of R_L there is a non-linearity in the output voltage V_L across the load, given by:

$$xV_S - V_L = V_SR_P(x^2 - x^3)/R_L$$

[6 marks]

Q3

The transistor shown in Figure Q3 has h_{ie}=1.25,h_{fe}=50, h_{oe}=20mS and negligible h_{re} at operating point of V_{CE} =12V, I_C= 1A, I_B= 20mA and V_{BE}= 0.5V.

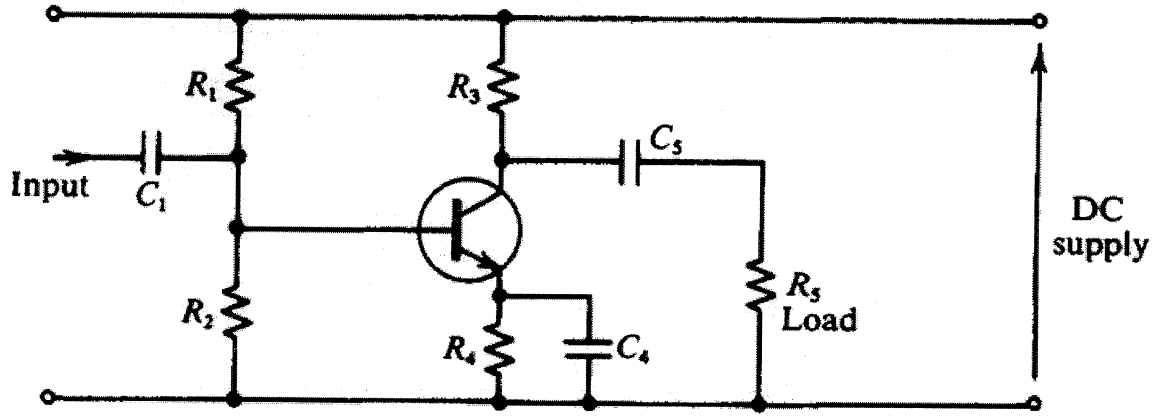


Figure Q3

(a) For a 25V supply, if the voltage across R_4 resistor is 1V and the current through the R_2 resistor is four times of biasing current ($4I_B$), calculate the values of R_1,R_2,R_3,$R_4$and R_5.

[8 marks]

(b) Find the optimum load and power developed in it by 15mA input current.

[6 marks]

(c) Calculate the stage efficiency and power gain. [6 marks]

Q4

(a) Figure Q4 (a) shows a MOSFET being used to switch on a high powered lamp from a light sensing circuit.

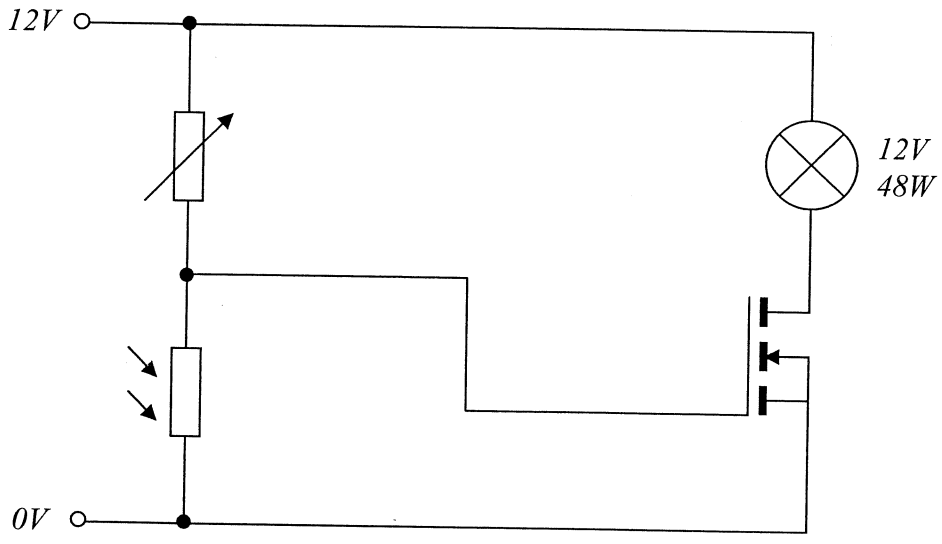


Figure Q4 (a)

An extract from the datasheet for the MOSFET is shown below:

V_{DS}/V (max)	V_{GS} /V (max)	I_D /A (max)	P_{TOT} /W (max)	g_M /S (typical)	$r_{DS_{ON}}$ /Ω
50	15	8	50	1.3	0.24

i Calculate the minimum value of voltage from the light sensing sub-system to allow the load to operate at it's rated power. [6 marks]

ii Calculate the power dissipated in the MOSFET when the lamp is operating at full power. [4 marks]

(b) The D-MOSFET amplifier shown in Figure Q4 (b) has $V_{GS(off)}$ = -2V, I_{DSS} = 4mA, g_{mo} = 2000μS. Find the output voltage of the amplifier.

[10 marks]

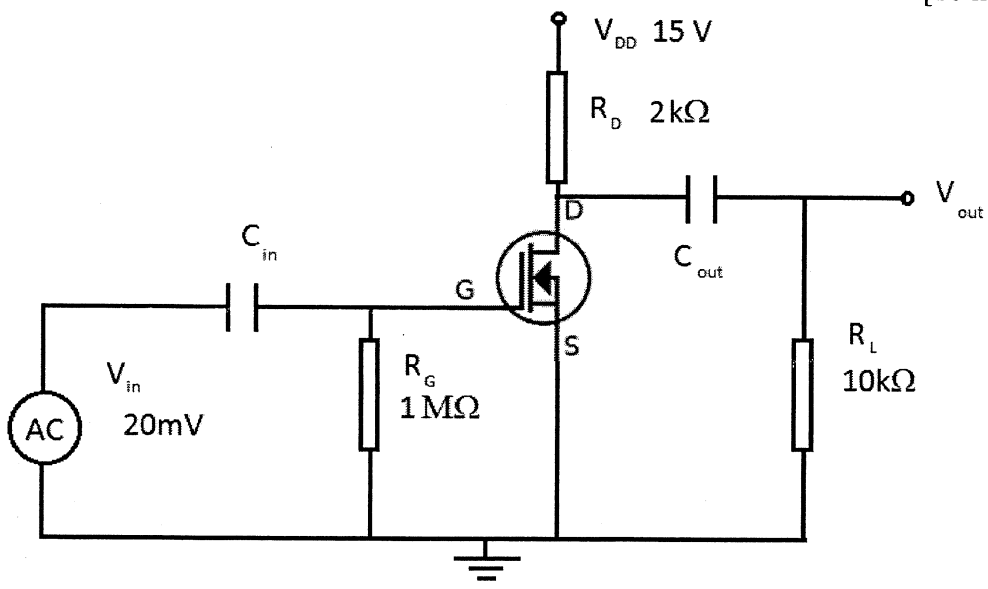


Figure Q4 (b)

Q5

An alternating voltage signal displayed on an oscilloscope screen is shown in Figure Q5 (a). The peak voltage is 6.0V and time base setting is 2ms/division.

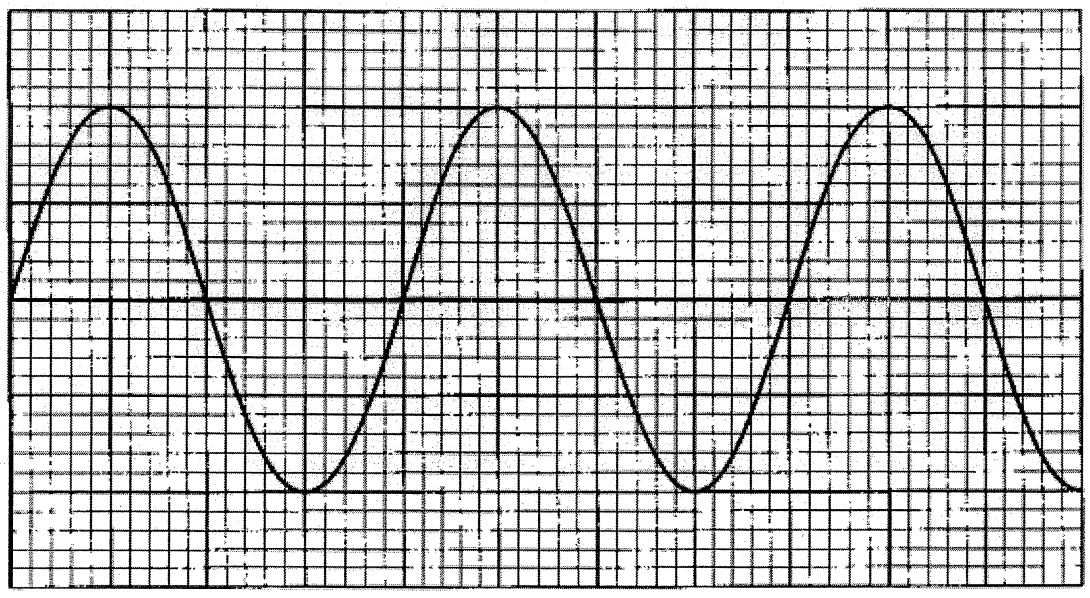


Figure Q5 (a)

(a) Find the frequency of the signal. [4 marks]

(b) This alternating voltage is used as the input voltage V_1 for the operational amplifier circuit shown in Figure Q5 (b). R_f is a variable resistor.

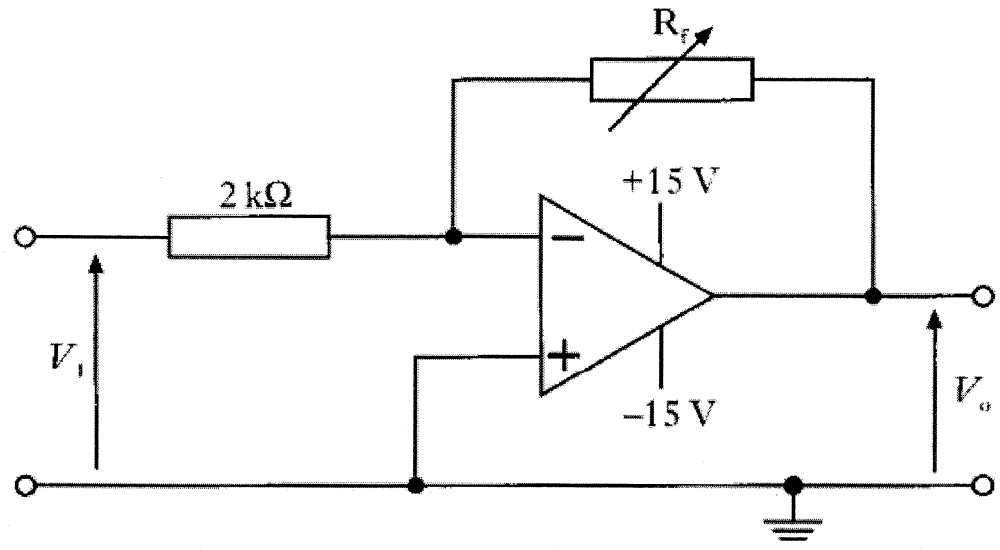


Figure Q5 (b)

i In what mode is the operational amplifier operating? [4 marks]

ii If $R_f = 3k\Omega$.

a. Sketch a output wave form of the amplifier V_o. Numerical values must be shown. [4 marks]

b. Calculate the output voltage V_o. [8 marks]

iii The resistance of resistor R_f is gradually increased from 3kΩ to 8kΩ. Describe the behavior of the output voltage V_o, indicating numerical values. [4 marks]

Q6

(a)

i Convert 1100101001010111_2 to Octal and Hexadecimal numbers. [2 marks]

ii Express the decimal number -54 in

a. Sign magnitude method
b. 1's compliment method
c. 2's compliment method [3 marks]

(b)

i State De Morgan's theorem for three Boolean variables A, B and C.[2 marks]

ii Define the following 2-input logic elements using truth tables.

a. NOR gate
b. NAND gate
c. Exclusive OR gate [3 marks]

iii Realize the following logic function using 2-input NOR gates.

$$f_1 = A.B + \overline{A}B$$

[2 marks]

(c)

i Draw a complete logic circuit of full adder and explain the operation of it. [4 marks]

ii Design a circuit to add a 3-bit binary number to another 3-bit binary number (eg:- 100 + 011 = 111) using appropriate adder circuits. (Clearly draw a circuit diagram and name the used components) [4 marks]

Q7

(a) Explain briefly the terms "Combinational-logic" and "Sequential-logic".[4 marks]

(b) Simplify the following logic functions using Boolean algebra.

i $[\overline{AB}(C + BD) + \overline{\overline{AB}}]C$

ii $\overline{A}BC + A\overline{BC} + \overline{\overline{A}BC} + A\overline{B}C + ABC$ [6 marks]

(c) Design a 3-bit **Gray Code** synchronous counter using JK Flip-Flop and logic gates. Show the state diagram, state table, K-map, logic expressions and the circuit implementation clearly. [10 marks]

Q8

AIron-safe has five locks, ***v, w, x, y***, and ***z***, all of which must be unlocked for the Iron-safe to open. The keys of the safe have been distributed among the five executives in the following manner:

- Mr. **A** has keys for locks ***v*** and ***x***
- Mr. **B** has keys for locks ***v*** and ***y***
- Mr. **C** has keys for locks ***w*** and ***y***
- Mr. **D** has keys for locks ***x*** and ***z***
- Mr. **E** has keys for locks ***v*** and ***z***

(a) Determine the minimum number of executives required to open the safe. [6 marks]

(b) Find all the combinations of executives that can open the safe. Write an expression for ***F(A,B,C,D,E)*** which specifies when the safe can be opened as a function of what executives are present. [8 marks]

(c) Who is the ***essential executive*** without whom the safe cannot be opened? [6 marks]

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