The Open University of Sri Lanka
Department of Electrical and Computer Engineering
Bachelor of Technology
ECX4230 – Fault Diagnosis in Electronic Circuits
Final Examinations – 2014/15 (Closed Book)

Date: 20.09.2015 Time: 09.30 – 12.30

Answer any five questions.

1. A differential amplifier circuit is shown in Figure 1.
The transistors Tr_1, Tr_2 and Tr_3 are of high gain and Tr_1 and Tr_2 are matched. The transistor Tr_4 is an n – channel JFET in which $I_D = 0.125(V_{GS}- V_P)^2$, where $V_P = -4V$. You may assume usual.

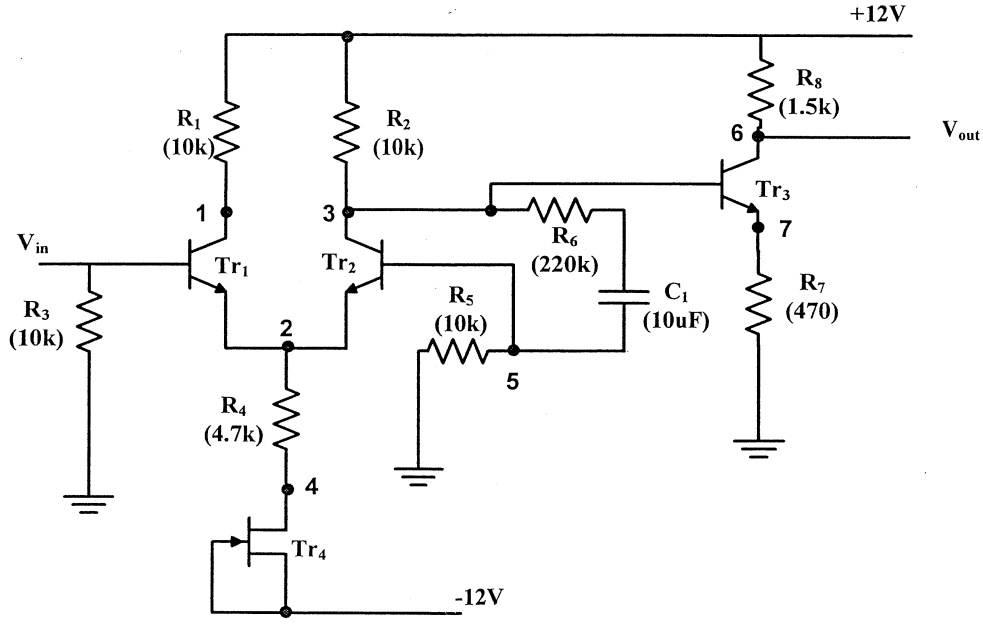


Figure 1

a. Calculate the test point voltages at no signal. (Do not assume a value for test point 6.) [7 marks]

b. A signal of 1kHz, 40mV peak to peak is given to the input and the resulting waveforms at the test points are observed using an oscilloscope. Draw the waveforms observed at the test point 6 to a common time scale with the input for the following settings.
   i. When the vertical amplifier of the scope is ac coupled
   ii. When the vertical amplifier of the scope is dc coupled [4 marks]

c. Following table shows test point voltages under faulty conditions. Identify the faulty component/s with the type of fault giving reasons. [9marks]

Case	1	2	3	4	5	6	7
A	12	0	12	0	0	2.93	2.83
B	- 0.5	- 0.6	3.16	-10	0	3.77	3.67
C	2	- 0.6	2	-10	0	12	0

2. A two stage preamplifier circuit is shown in figure 2. The transistors are of silicon and the current gains of Tr_1 and Tr_2 are 75 and 50 respectively.

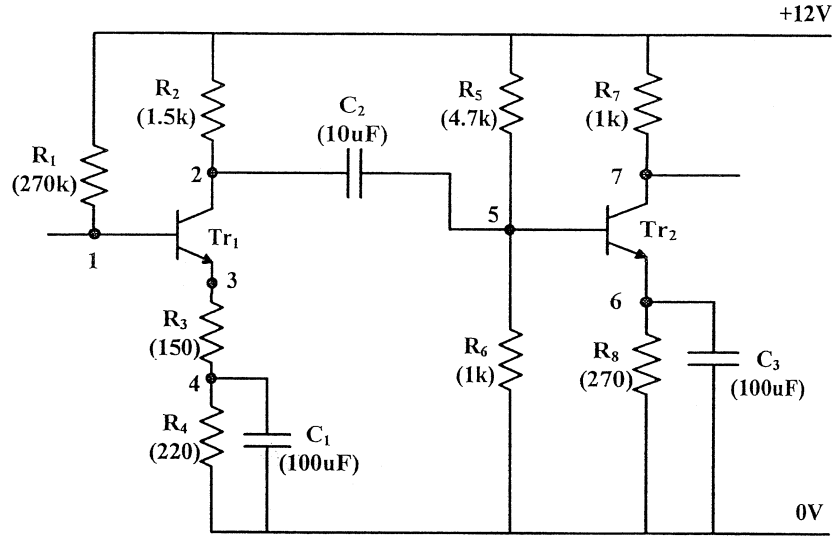


Figure 2

a. Calculate the test point voltages at no signal. (Do not assume a value for test point 7.) [7 marks]

b. When 1kHz sine wave is given to the input, the signal at test point 7 becomes 2V peak to peak when the signal at test point 5 is 9.7 mV peak to peak. Find the amplitude and the phase of the output signal, if the input signal is 2mV peak to peak. [4 marks]

c. Following is a table of dc test point voltages measured with DVM under faulty conditions of the circuit. When the signal voltages are observed, input is given a 1kHz, 2mV peak to peak sine wave test signal. Identify the faulty component/s stating the fault type and reasons to justify your answer. [9marks]

Case	1	2	3	4	5	6	7	other
A	1.69	7.70	1.09	0.65	2.02	1.42	6.85	8.12 mVp-p at 5 and 1.67 Vp-p at 7
B	1.69	7.70	1.09	0.65	3.11	2.51	2.71	Negative going pulses clipped
C	1.69	7.70	1.09	0.65	0.97	0.37	12	No out put

3.

a. State the advantages and disadvantages of linear regulators over switch mode regulators. [3 marks]

b. A DC power supply is shown in figure 3.

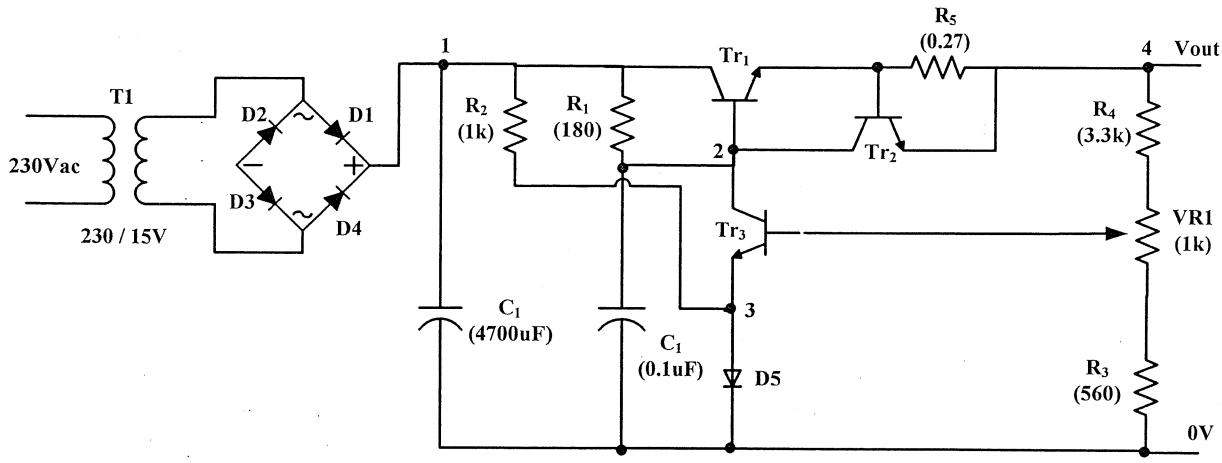


Figure 3

i. Calculate the range of the output voltage. [3 marks]

ii. Is it possible to use this supply for 27 W load at 9V? if not show how you are going to modify the circuit to achieve this. [4 marks]

iii. Following table shows the voltages at the test points under faulty conditions. Find the faulty component/s with fault type giving reasons. Assume VR1 is set to give the maximum output. [10 marks]

Case	1	2	3	4
A	15.00	14.80	0.60	14.20
B	15.00	6.96	0.60	6.36
C	15.00	5.81	0	5.21
D	15.00	14.80	0	14.20
E	15.00	15.00	0.60	0

4.

a. Explain the use of logic probe, logic pulser and current tracer. [3 marks]

b. What are the limitations of logic probe? [2 marks]

c. Consider the logic circuit shown in figure 4.

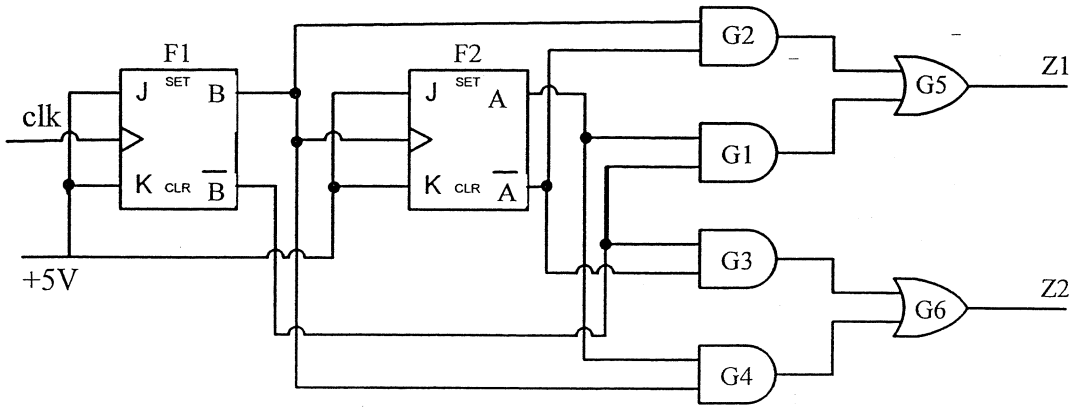


Figure 4

i. The JK flip-flops are of positive edge trigger type and the clock pulses are given after resetting the flip-flops. Draw the timing diagram to show the clock and the signals at A and B. [3 marks]

ii. Tabulate the number of clock pulses with A_t, B_t, A_{t+1}, B_{t+1}, Z1 and Z2. 't' and 't+1' are the instances before and after the clock pulse respectively. [6 marks]

iii. Following table shows the logic status of Z1 and Z2 observed by a logic probe. With the clock pulses under faulty conditions. Assume the flip-flops are cleared before applying the clock pulses. Find the faulty component/s with the type of fault. [6 marks]

Clock pulse		1	2	3	4
Case A	Z1	0	1	0	1
	Z2	1	0	1	0
Case B	Z1	0	0	1	1
	Z2	0	1	0	0
Case C	Z1	1	1	1	1
	Z2	1	1	0	0

5. Circuit shown in figure 5 uses a Schmitt trigger with a JFET. The JFET starts to conduct when $V_{GS} > -1$ and when the JFET is 'ON', its V_{DS} is 1V.

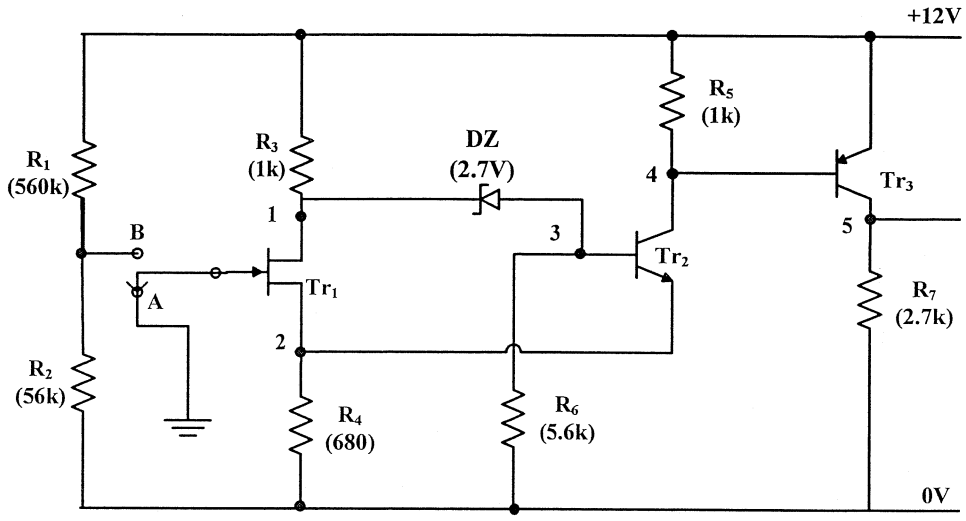


Figure 5

a. Calculate the threshold voltages of V_3 at which the output of the circuit will change. [5 marks]

b. Calculate the test point voltages for the two states of the output. [Note: Assume the $V_{CE\ sat}$ for the two transistors are 0.2V] [6 marks]

c. Explain the operation of the circuit when the switch is connected to position B.

d. Following table shows three fault cases with the measured test point voltages when the switch is at position A. State the faulty component/s with fault type giving reasons. [9 marks]

Case	1	2	3	4	5
A	10.08	6.78	7.38	2.03	0
B	6.28	3.52	4.12	11.40	11.80
C	6.54	3.24	3.84	12.00	0

6.

a. What is used to match the input impedance of the RF amplifier of a TV to that of an antenna? [2 marks]

b. Show in a block diagram how the TV signal is processed after extracting sound in a color receiver. [4 marks]

c. What are the signals used to ensure the lines and the frames in their proper places? [3 marks]

d. Explain how the detected Y and color component signals in a PAL receiver are used to drive the picture tube. [4 marks]

e. Name the sections preceding to the IF stage of a PAL color receiver and explain their function briefly. [3 marks]

f. In a defective TV receiver, sound signal and the raster is received but no picture. What could be the faulty sections? Explain how you are going to locate the fault using an oscilloscope [4 marks]

7.

a. A pnp transistor is tested using an analog multi-meter set to 10 ohms range. Indicate the meter response in the meter as 'low Ω','high Ω' and 'zero Ω' [4 marks]

Black probe (-)	Red probe (+)	Response
base	emitter	
base	collector	
emitter	base	
emitter	collector	
collector	base	
collector	emitter	

b.

i. State four triggering modes of a traic. [4 marks]

ii. Traic parameters are given below. The circuit shown in figure 7 is used to test a suspected traic having the above data.

Repetitive peak off state voltage 400V
On state current (r.m.s) 8A
Peak gate voltage 10V
Peak gate current 2A
Min. gate trigger current 50mA
Min. gate trigger voltage 2V
Peak on state voltage 1.5V
Holding current 5mA
Latching current 50mA

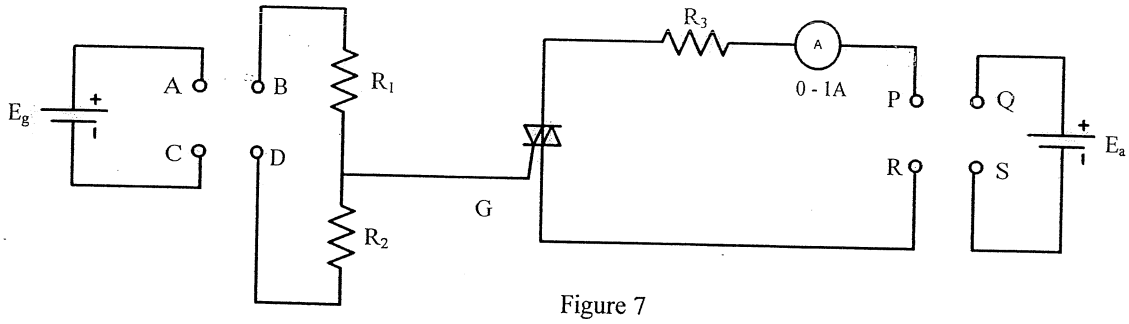


Figure 7

I. Find suitable values for E_g, E_a, R_1,R_2,R_3 [7 marks]

II. State the steps that you will follow to test the traic and the observations expected. [5 marks]

8.

a. An amplifier of open loop A_0 is supplied with positive feedback. If the feedback ratio is β, find an expression for the overall gain. [3 marks]

b. What will happen when $\beta A_0 = 1$? [2 marks]

c. The circuit shown in figure 8 is a blocking oscillator.

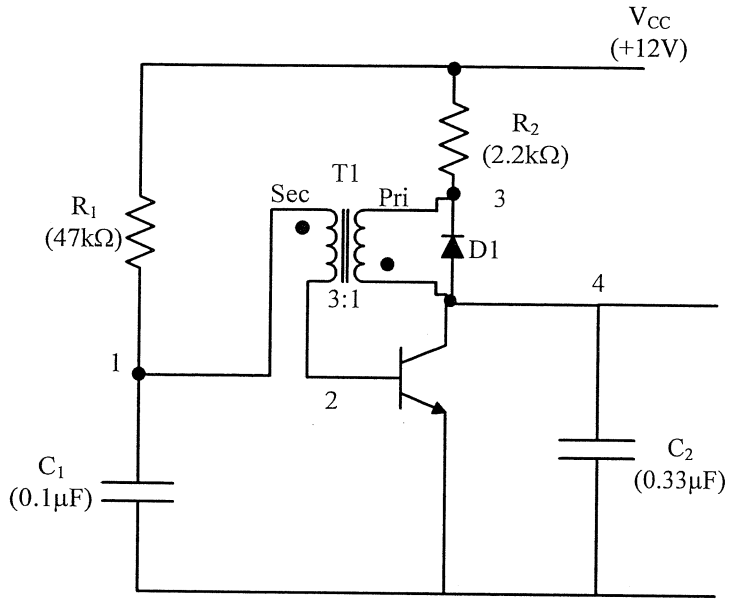


Figure 8

i. Explain the operation and, sketch the waveforms at the output. [4 marks]

ii. What is the function of D_1? [2 marks]

iii. State the faulty component/s and the fault type with reasons for the following. [9 marks]

Case	1	2	3	4	Symptom
A	0	0	12	12	No output
B	0.7	0.7	0.1	0.1	No output
C	9.7	0	12	12	No output